DESCRIPTION

AP8358 combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications.

AP8358 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). Excellent EMI performance is achieved with proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20kHz is minimized in the design and audio noise is eliminated during operation.

The AP8358 is available in DIP7 package.

ORDERING INFORMATION

Package Type	Part Number	
DIP7 SPQ: 50psc/Tube	P7	AP8358P7U
		AP8358P7VU
Note	V: Halogen free Package U: Tube	
AiT provides all RoHS products		

FEATURES

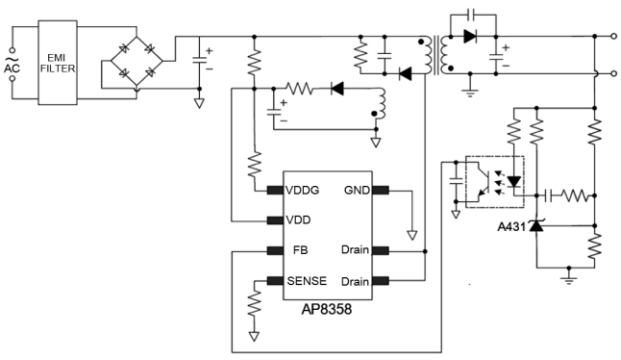
- Power on Soft Start Reducing MOSFET V_{DS} Stress
- Frequency shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 50kHz Switching Frequency
- Internal Synchronized Slope Compensation
- Low V_{DD} Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input Good Protection Coverage With Auto Self-Recovery
  - V_{DD} Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
  - Line Input Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range
  - Overload Protection (OLP)
  - Over Voltage Protection (OVP)

APPLICATION

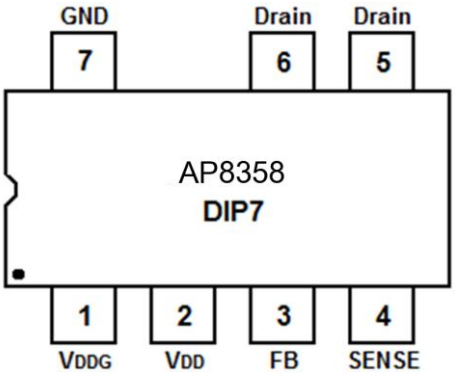
Offline AC/DC flyback converter for

- Battery Charger
- PDA power supplies
- Digital Cameras and Camcorder Adaptor
- VCR, SVR, STB, DVD&DVCD Player SM
- Set-Top Box Power
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

TYPICAL APPLICATION



PIN DESCRIPTION



DIP7, P7

Top View

Pin #	Symbol	I/O	Function
1	V_{DDG}	P	Internal Gate Driver Power Supply
2	V_{DD}	P	IC DC power supply Input
3	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
4	SENSE	I	Current sense input
5	Drain	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer
6	Drain	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer
7	GND	P	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Drain Voltage (off state)		-0.3 ~ 650	V
VDD Voltage	V_{DD}	-0.3 ~ 30	V
VDD-G Input Voltage	V_{DDG}	-0.3 ~ 30	V
VDD Clamp Continuous Current	V_{DD}	10	mA
FB Input Voltage		-0.3 ~ 7	V
SENSE Input Voltage		-0.3 ~ 7	V
Min/Max Operating Junction Temperature	T_J	0 ~ 125	℃
Min/Max Storage Temperature	T_{stg}	-25 ~ 150	℃
Lead Temperature (Soldering,10secs)		260	℃
Ambient Operating Temperature		-25 ~ 85	℃
Thermal Resistance from Junction to case	θ_{JC}	15	℃/W
Thermal Resistance from Junction to ambient *	θ_{JA}	75	℃/W

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* θ_{JA} is measured with the PCB copper area of approximately 1 in^2 (Multi-layer). That need connect to exposed pad.

OUTPUT POWER TABLE

Product	230VAC±10%	85-264VAC	Package
	Open Frame	Open Frame	
AP8358	15W	12W	DIP7

* Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50℃ ambient.

ELECTRICAL CHARACTERISTICS

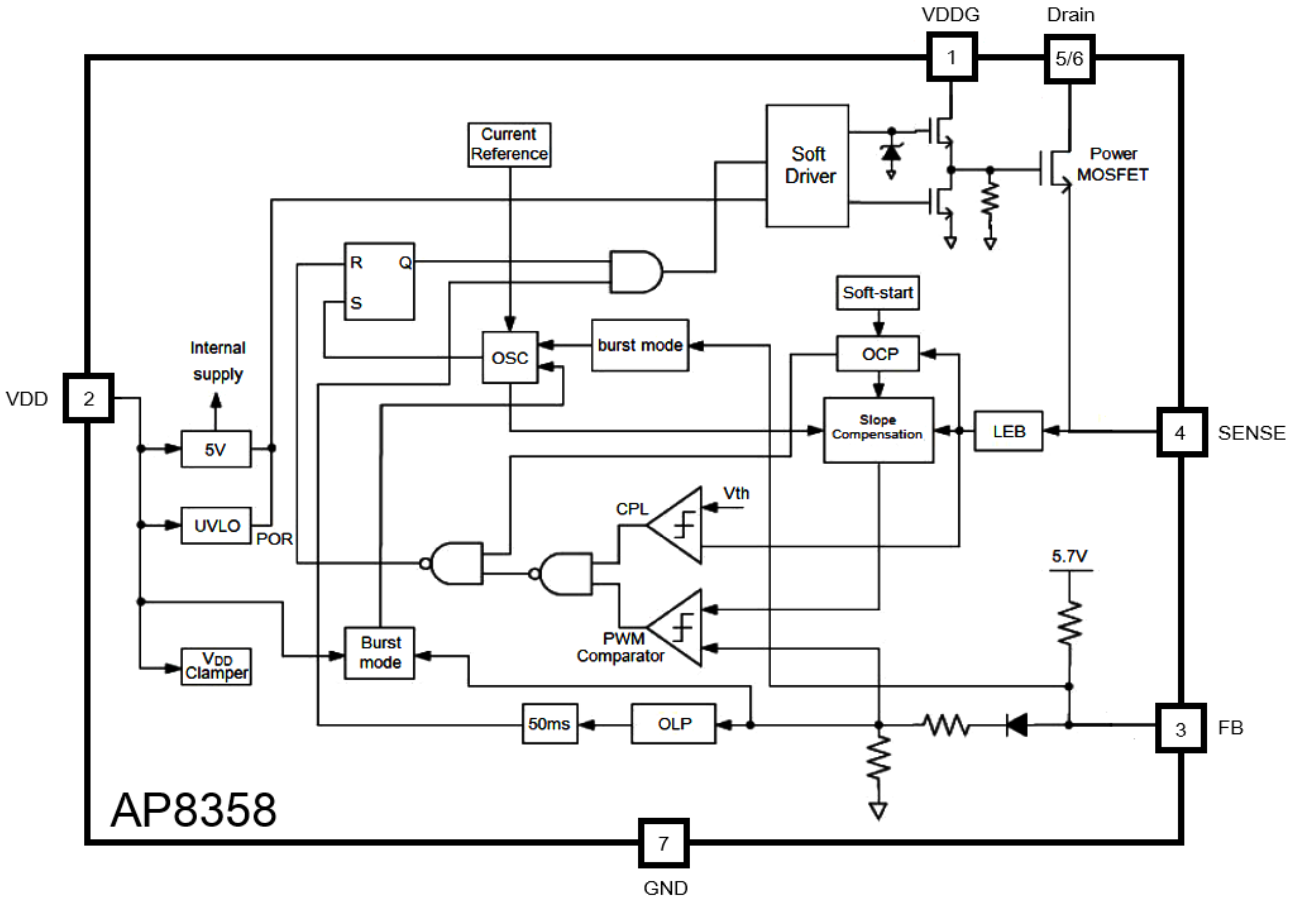
T_A = 25℃, V_{DD}=V_{DDG}=16V, if not otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})						
V_{DD} Startup Current	I _start up	V_{DD}=14.5V, Measure Leakage current into V_{DD}	-	5	20	uA
Operation Current	I_op	V_{FB}=3V	-	2.1	-	mA
V_{DD} Under Voltage Lockout Enter	UVLO(ON)		8.7	9.3	10.7	V
V_{DD} Under Voltage Lockout Exit	UVLO(OFF)		14.8	15.3	16.0	V
V_{DD} Zener Clamp Voltage	V_{DD}_Clamp	I_{DD}=10mA	-	30	-	V
Over Voltage Protection Threshold	OVP(ON)	CS=0V,FB=3VRamp up V_{DD} until gate clock is off	27	28.8	30	V
Feedback Input Section (FB Pin)						
V_{FB} Open Loop Voltage	VFB _Open		5.4	5.6	6	V
FB Pin Short Circuit Current	IFB _Short	Short FB pin to GND and measure current	-	1.45	-	mA
Zero Duty Cycle FB Threshold Voltage	VTH_0D		-	1.23	-	V
Power Limiting FB Threshold Voltage	VTH_PL		-	3.5	-	V
Power Limiting FB Debounce Time	TD_PL		-	50	-	ms
Input Impedance	ZFB_IN		-	4	-	kΩ
Current Sense Input (Sense Pin)						
Soft start time			-	4	-	ms
Leading Edge Blanking Time	T_ blanking		-	270	-	ns
Input Impedance	ZSENSE_ IN		-	40	-	kΩ
Over Current Detection and Control Delay	TD_ OC	From over current occurs till the gate drive output start to turn off	-	120	-	ns
Internal Current Limiting Threshold Voltage	VTH_ OC	FB=3.3V	-	0.95	-	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator						
Normal Oscillation Frequency	Fosc		43	48	53	kHz
Frequency Temperature Stability	Δf_ Temp		-	5	-	%
Frequency Voltage Stability	Δf_ V_{DD}		-	5	-	%
Maximum Duty Cycle[NOTE1]	D_ max	FB=3.3V, CS=0V	70	80	90	%
Burst Mode Base Frequency	F_ Burst		-	22	-	kHz
Power MOSFET Section						
MOSFET Drain-Source Breakdown Voltage	BV-DSS		600	-	-	V
Rdson*	On Resistance		-	4	-	Ω
Frequency						
Frequency Modulation Range/Base Frequency	Δ_V_{DD}		-5	-	+5	%

* Guaranteed by design.

BLOCK DIAGRAM



DETAILED INFORMATION

Operation Description

The AP8358 is a low power off-line SMPS switcher optimized for off-line flyback converter applications in sub 15W power range. The 'Extended burst mode' control greatly reduces the standby power consumption and help the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of AP8358 is designed to be very low so that V_{DD} could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a 2M Ω, 1/8W startup resistor could be used together with a V_{DD} capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of AP8358 is low at 2mA.Good efficiency is achieved with AP8358 low operating current together with the 'Extended burst mode' control features.

Soft Start

AP8358 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as V_{DD} reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.95V. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in AP8358. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition.

The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drop below burst mode threshold level and device enters Burst Mode control. The gate drive output switches only when V_{DD} voltage drop below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency of AP8358 is internally fixed at 50kHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in AP8358 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Drive

The internal power MOSFET in AP8358 is driven by a dedicated gate driver for power switch control.
Too weak the gate drives strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

Protection Controls

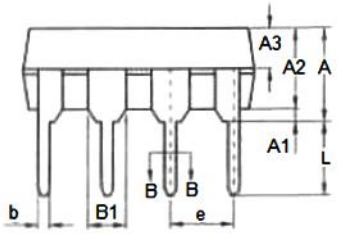
Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

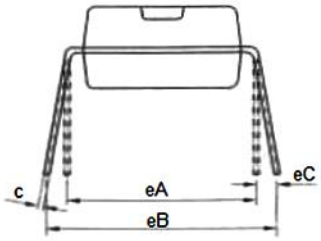
Protection (OLP) and over voltage clamp, Under Voltage Lockout on V_{DD} (UVLO).
With proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.
At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher. Switcher restarts when V_{DD} voltage drop below UVLO limit.

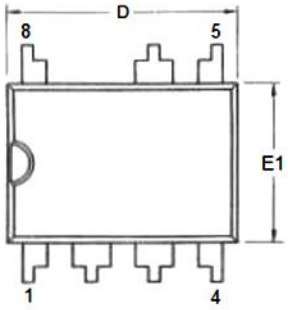
V_{DD} is supplied by transformer auxiliary winding output. It is clamped when V_{DD} is higher than 30V.
The output of AP8358 is shut down when V_{DD} drop below UVLO_ON limit and Switcher enters power on start-up sequence.

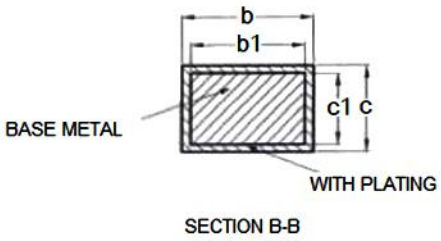
PACKAGE INFORMATION

Dimension in DIP7 (Unit: mm)









Symbol	Min.	Max.
A	3.600	4.000
A1	0.510	-
A2	3.000	3.400
A3	1.550	1.650
b	0.440	0.530
b1	0.430	0.480
B1	1.520 BSC	
c	0.250	0.310
c1	0.240	0.260
D	9.050	9.450
E1	6.150	6.550
e	2.540 BSC	
eA	7.620 BSC	
eB	7.620	9.300
eC	0.000	0.840
L	3.000	-

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