DESCRIPTION

The AP8275 consists of an integrated current mode Pulse Width Modulator (PWM) controller and high voltage start circuit, specifically designed for a high performance off-line converter with minimal external components. QR-PWM, QR-PFM, Burst-mode operation and low consumption device help to meet the standby energy saving standards and achieve higher efficiency. Excellent EMI performance is achieved by frequency modulation and soft driver technique. The AP8275 offers completed and excellent protections including Brown-in/out, AC Line OVP, X-cap discharge, output over voltage protection, external over temperature protection. Cycle-by-Cycle current limiting, over load protection.

The AP8275 is available in SOP7 package

ORDERING INFORMATION

Package Type	Part Number			
SOP7	1.47	AP8275M7R-Y		
SPQ: 4,000pcs/Reel	M7	AP8275M7VR-Y		
	Y: Fun	ction Type		
	A: AC Line OVP			
Note	B: E	Brown-in/out		
	V: Halogen free Package			
	R: Tape & Reel			
AiT provides all RoHS products				

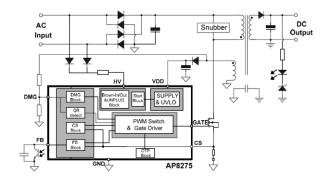
FEATURES

- Internal HV Start-up Circuit
- Multi-mode operation to achieve higher efficiency
- Adaptive PWM switching frequency 65/85kHz
- AC Brown-in/out protection(AP8275-B)
- AC Line over voltage protection(AP8275-A)
- X-cap discharge function (Pass IEC62368-1:2014 certification)
- No-load consumption power < 50mW @230VAC
- Proprietary Frequency Jitter for EMI
- V_{DD} Operating voltage range 8~40V
- Adjustable AC Line Input Compensation
- Excellent Protection Coverage
 - Over Temperature Protection (OTP)
 - Output over voltage protection
 - Cycle-by-cycle Over Current Protection (OCP)
 - Output Open/short Protection
 - Patented DMG resistor short protection (Latch)
 - Secondary Rectifier Short Protection
 - Over Load Protection (OLP)
- Available in SOP7 Package

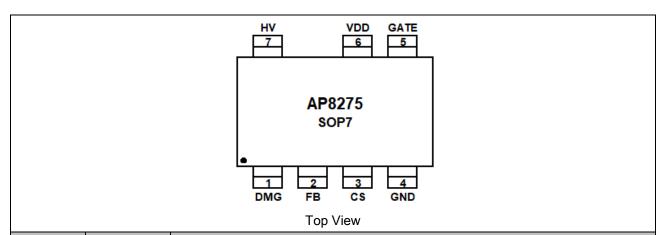
APPLICATION

- Stand-by power
- Open-frame SMPS
- Adaptor

TYPICAL APPLICATION



PIN DESCRIPTION



Pin#	Symbol	Function		
1	DMG	Demagnetization pin. Input and output voltage detection by the voltage divider		
I	DIVIG	resistors.		
2	FB	Voltage feedback. By connecting an opto-coupler to close the control loop and		
	ГБ	achieve the regulation.		
3	CS	Current Sense Input		
4	GND	Ground		
5	GATE	Totem-pole gate drive output for the power MOSFET.		
6	V_{DD}	Positive Supply voltage Input		
		High voltage start pin.		
7	HV	High voltage startup, X-cap discharge and AC Brown-in/out protection/ AC Line		
		over voltage protection are realized by connecting diodes to AC input.		

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ABSOLUTE MAXIMUM RATINGS

Supply voltage Pin V _{DD}		-0.3V ~ 43V
FB, CS, DMG Pin		-0.3V ~ 7V
GATE Pin		-0.3V ~ 15V
HV Pin		-0.3V ~ 800V
Operating Junction Temperature°C		-40°C~ 150°C
Storage Temperature Range		-55°C~ 150°C
Lead Temperature (Soldering, 10Secs)		260°C
Package Thermal Resistance	SOP7	80°C/W
HBM ESD Protection ^{NOTE1}		±4.0kV
MM ESD ProtectionNOTE2		300V

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE1: Test standard: JEDEC JS-001-2014。 NOTE2: Test standard: JESD22-A115C-2010

TYPICAL POWER

Part Number	Input Voltage	Adapter ^{NOTE3}		
AP8275	90-265 V _{AC}	120W		

NOTE3: Typical output power is tested in an adapter at 40°C ambient temperature, with enough cooling conditions.

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ELECTRICAL CHARACTERISTICS

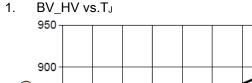
 T_A =25°C, V_{DD} =15V, unless otherwise specified

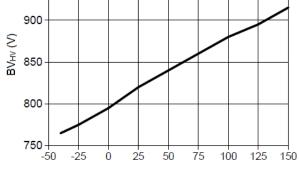
T _A =25°C, V _{DD} =15V, unless otherw Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
HV section	- Cyllibol	Conditions	14/11/17	· 3P.	I III AX.	Offic
Break-Down Voltage	BV _{HV}	I _{HV} =250μA	800	830	_	V
			1		2	
Start Up Charging Current	I_HV	V _{DD} =V _{DDoff} -1, HV=500V	-	1.5		mA
Off-State Current	loff	HV =500V	5	18	30	μA
X-Cap Discharge Voltage	V_UNPLUG		-	35	-	V
Power Down Detection	td_UNPLUG		_	60	_	ms
Enabling Duration						
HV section- AC Line OVP AP827	′5-A	T			1	
HV OVP Voltage	V_OVP	DC Level	439	460	481	V
HV OVP Hysteresis Voltage	V_OVP_hys		-	27	-	V
HV section- Brown/in out AP827	5-B					
Brown In Voltage	V_BNI		108	115	122	٧
Brown In Enabling Duration	td_BNI		-	150	-	μs
Brown Out Voltage	V_BNO		90	102	109	V
Brown Out Enabling Duration	td_BNO		-	60	-	ms
V _{DD} Supply Voltage Section	•					
V _{DD} Start Up Threshold	V_{DDon}		18.3	19.3	20.3	V
V _{DD} Under Voltage	.,		_			
Shutdown Threshold	V_{DDoff}		7	8	9	V
V _{DD} OVP Voltage	V _{DDovp}		38	40.5	43	V
De-Bounce time of V _{DD} OVP	11.01/5					
Voltage	td_OVP		-	80	-	μs
V _{DD} Threshold for Continuous						
Work Under BM	Vhold-up		-	10	-	V
V _{DD} Restart Voltage	V _{Restart}		_	4	-	V
V _{DD} Supply Current Section	1	<u>I</u>	l		<u> </u>	
Operating Supply Current,						
Switching	I _{VDD0}	V _{FB} =3.5V,CS=0.3V	1	1.5	3.0	mA
Operating Supply Current,						
Under Burst Mode	IVDD1	V _{FB} =0.5V,CS=0.3V	0.1	0.65	1.5	mA

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Operating Supply Current, With Protection Tripping	IVDD_Fault	After OVP	0.1	0.8	1.5	mA
OSCILLATOR Section	1	1				l .
		I _{DMG} >330μA	60	65	70	kHz
Switching Frequency	fosc	I _{DMG} <330μA	77	85	92	kHz
Burst Mode Frequency	fosc_BM		-	22	-	kHz
Jitter Frequency	f_jitter		-	30	-	Hz
Frequency Modulation range	Δfosc		-	±6	-	%
FB Section	l	1		I		l
FB Loop Voltage	V _{FB}		4.8	5.2	5.4	V
FB Short Current	I _{FB_SHORT}		-	0.2	-	mA
Maximum Duty Cycle	Dmax		70	80	90	%
		I _{DMG} >330μA	_	2.5	-	V
Green Mode Entry Voltage	V _{FB_PFM}	I _{DMG} <330μA	-	1.8	-	V
Burst Mode Entry Voltage	V _{FB_BM_L}		-	1.15	-	V
Burst Mode Ending Voltage	V _{FB_BM_H}		-	1.25	-	V
OLP Threshold Voltage	Vth_OLP		4.1	4.4	4.7	V
OLP De-Bounce Time	td_OLP		-	60	-	ms
CURRENT SENSE SECTION		1		I		
Soft-Start Time	t _{SS}		-	8	-	ms
Leading Edge Blanking Time	t _{LEB}		-	400	-	ns
Internal Current Limiting Threshold Voltage	Vth_OCP		0.72	0.75	0.78	V
Threshold Voltage of						
Secondary Rectifier Short	V_{DSP}		_	1.1	_	V
Protection	- 501					
De-Bounce Time of SRCP	td_DSP		_	7	-	Cycles
CS OTP Threshold Voltage	V_CSOTP		0.78	0.8	0.82	V
CS OTP De-Bounce Time	td_CSOTP		-	48	_	ms
DMG Section						
DMG OVP Voltage	V_{DMG_OVP}		2.7	3	3.3	V
De-Bounce Time of DMG	(1.50)/5			_		
OVP	td_DOVP		-	7	-	Cycles
Maximum Hold Time	thold		-	5	1	us

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Minimum Duty Cycle of Slope	Destre Olema	f C[]- -		25		0/
Compensation	Duty_Slope	fosc=65kHz	-	35	-	%
Minimum Turn ON Time	ton_max		-	12	-	us
GATE Section						
Output Low Level	V_{OL}		-	-	1	V
Output High Level	V _{OH}		6	-	-	V
Output Clamp Voltage Level	V_clamping	CS=0.3V,FB=3V	-	12	-	V
Outsid Bising Time	4	1.2V~10.8V		00		
Output Rising Time	t_r	@C _L =1000pF	_	60	-	ns
Output Falling Time	1.5	10.8V~1.2V	-	20	-	ns
Output Falling Time	t_f	@C _L =1000pF				
Thermal section						
Thermal Shutdown Temperature	T _{SD}		130	145	-	°C
Thermal Shutdown Hysteresis	T _{HYST}		-	30	-	$^{\circ}$

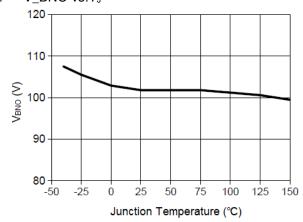
TYPICAL PERFORMANCE CHARACTERISTICS



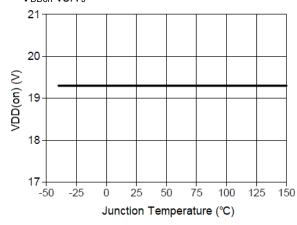


Junction Temperature (°C)

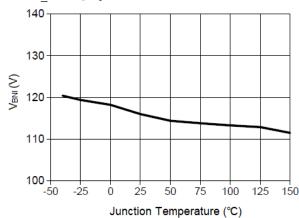




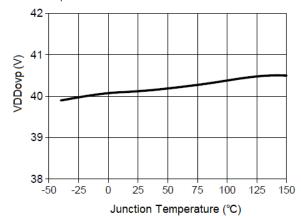
5. V_{DDon} vs.T_J



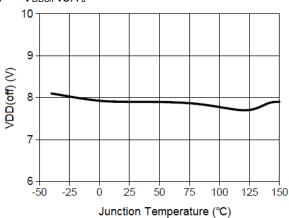
V_BNI vs.T_J

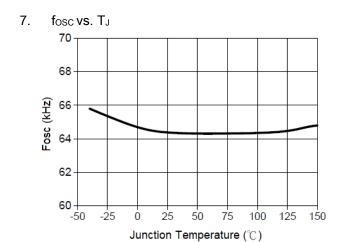


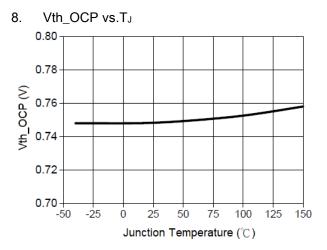
4. V_{DDovp} vs. T_J

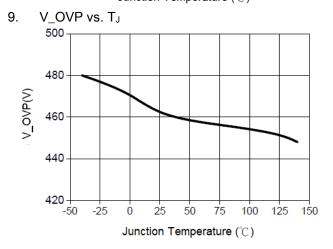


6. V_{DDoff} vs.T_J

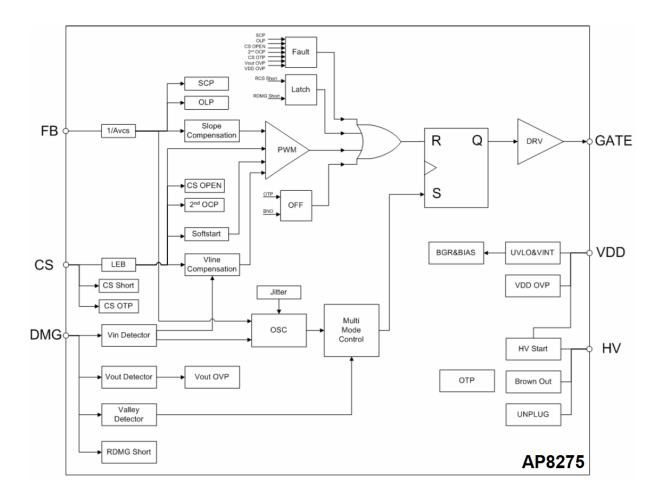








BLOCK DIAGRAM



DETAILED INFORMATION

Startup

At start up, the internal high-voltage current source supplies the internal bias and charges the external V_{DD} capacitor. When V_{DD} reaches V_{DDon} , the device starts switching and the internal high-voltage current source stops charging the capacitor. After start up, the bias is supplied from the auxiliary transformer winding.

Soft-start up

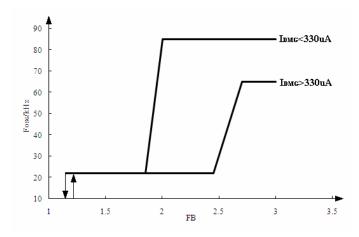
In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and prevent the transformer turning into the saturation state. Typically, the duration of soft-start is 8ms.

Oscillator

The switching frequency of AP8275 is internally fixed. When the input voltage is high (I_{DMG}>330uA), the frequency is 65kHz. When the input voltage is low (I_{DMG}<330uA), the frequency is 85kHz. The AP8275 can ease the design of the transformer by increasing the switching frequency.

PFM mode

PFM operation helps to meet the standby energy saving standards and achieve higher efficiency. When FB is less than V_{FB_PFM}, the AP8275 enter PFM. Lighter the load, less the switching frequency. The minimum switching frequency is closed at fosc_BM.



Quasi-Resonant switching

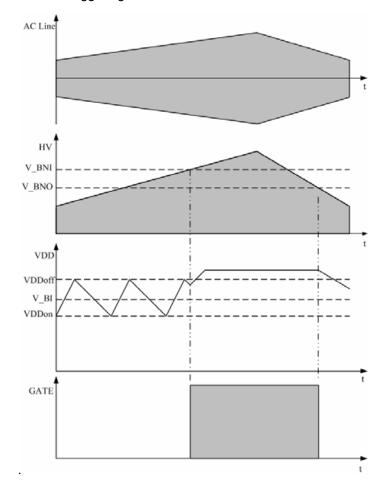
The AP8275 can calculate the frequency of the Lm and Clump oscillator. The valley detection is realized by DMG pin to achieve accurate valley opening, and improve the conversion efficiency under DCM.

Burst-mode operation

The AP8275 enters burst-mode operation in order to minimize the power dissipation in standby mode. As the load decreases, the feedback voltage decreases. When the voltage on FB pin falls below V_{FB_BM_L} (1.15V typically), the device enters burst mode and power MOSFET stops switching. It can be switched on again once the voltage on FB pin exceeds V_{FB_BM_H}.

Brown-in/out protection- AP8275-B

The AP8275-B features Brown-in/out function on HV pin. When HV < V_BNO , GATE pin will remain off even when the V_{CC} already reaches V_{DDon} . It therefore forces the V_{DD} hiccup between V_{DDon} and V_{DDon} . Unless the next V_{DDon} is tripped and the line voltage rises over V_BNI , GATE pin will start switching. A hysteresis is implemented to prevent the false-triggering.



AC Line OVP- AP8275-A

AP8275-A integrates input voltage detection module to realize AC Line OVP function. When the HV voltage is higher than V_OVP, the GATE output will stop switching; when AC Line Voltage decreases, AP8275-A detects that the HV voltage is less than V_OVP-V_OVP_hys, and the GATE output will start switching again.

Gate driver

The internal power MOSFET in the AP8275 is driven by a dedicated gate driver for power switch control. A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

Over Load Protection (OLP)

Overload is defined as the load current exceeding a pre-set level due to an accident event as a fault. If FB exceeds Vth_OLP for more than td_OLP (de-bounce time of OLP), the protection circuit should be activated to protect the SMPS.

X-cap discharge

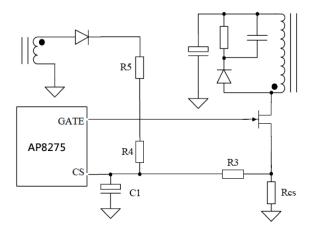
The AP8275 features X-cap discharge function on HV pin. When the AC input is unplugged, the AP8275 will discharge the X-cap until the voltage is under the safety range. This function has been certified by IEC 62368-1:2014

Internal Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the feedback voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Line Input Compensation

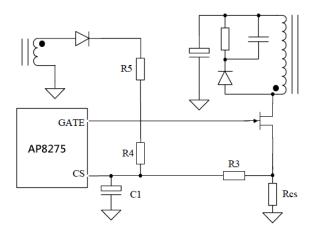
The AP8275 offers Line Input Compensation; this feature improves the power limit constant output. The AP8275 detects the input voltage across DMG pin and generate the compensated current. Thus the compensated current can be calculated as I_{LC}=K*I_{DMG}, where K is the compensated coefficient. ILC multiplied R3 equals the compensated voltage that can limit the pulse-by-pulse current.



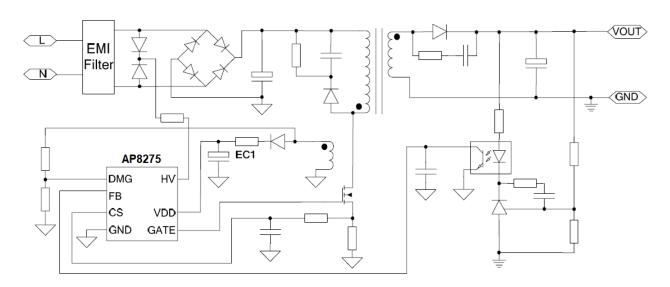


Over Temperature Protection

Both an internal OTP circuit and an external OTP circuit are embedded inside the AP8275 to prevent the system from hot damage. If the temperature exceeds about 145°C, OTP fault is activated. Simultaneously, an NTC resistor is implemented to sense whether there is any hot-spot of power circuit. If the voltage exceeds the external OTP trip level VCS>V_CSOTP (typical 0.8V), an internal counter has been added to prevent incorrect OTP detection. However, if td_CSOTP of subsequent OTP events are detected, the external OTP protection is tripped.



Typical Application

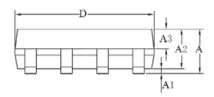


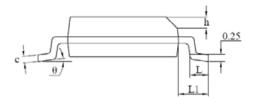
Component Parameter and Layout Considerations:

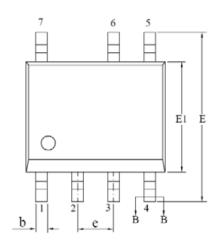
1. V_{DD} capacitor EC1 should be placed at the nearest place from the V_{DD} pin and the GND pin.

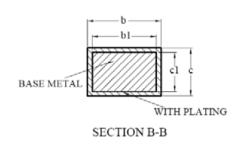
PACKAGE INFORMATION

Dimension in SOP7 (Unit: mm)









Symbol	Min	Max	
Α	-	1.75	
A1	0.10	0.225	
A2	1.30	1.50	
A3	0.60	0.70	
b	0.39	0.48	
b1	0.38	0.43	
С	0.21	0.26	
c1	0.19	0.21	
D	4.70	5.10	
Е	5.80	6.20	
E1	3.70	4.10	
е	1.27 BSC		
h	0.25	0.50	
L	0.50	0.80	
L1	1.05 BSC		
θ	0°	8°	

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