DESCRIPTION

The A7230 is a monolithic synchronous buck regulator. The device integrates 100mΩ MOSFETS that provide 3A continuous load current over a wide operating input voltage of 4.75V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on. In shutdown mode, the supply current drops below 1μA.

This device, available in an SOP8 package, provides a very compact system solution with minimal reliance on external components.

The A7230 is available in PSOP8 package.

ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ : 4,000pcs/Reel	MP8	A7230MP8R
		A7230MP8VR
Note	R: Tape & Reel V: Halogen free Package	
AiT provides all RoHS products		

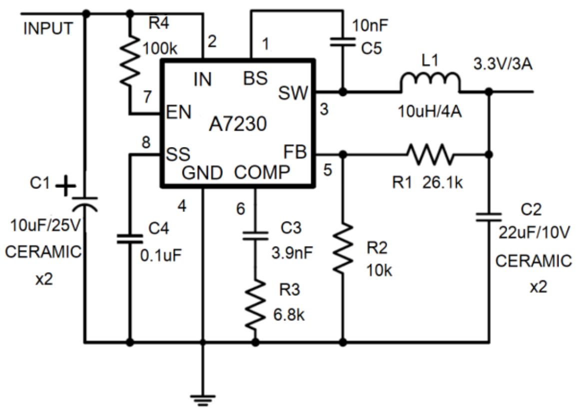
FEATURES

- 3A Output Current
- Wide 4.75V to 18V Operating Input Range
- Integrated 100mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 15V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 370kHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Available in PSOP8 package

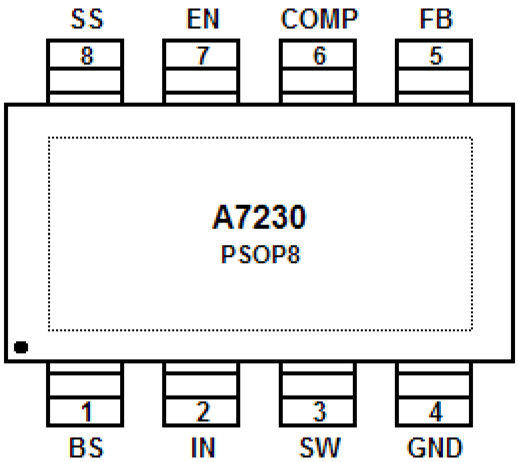
APPLICATION

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION



PIN DESCRIPTION



Top View

Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01μF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 18V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground (Connect Exposed Pad to Pin 4).
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.925V. See Setting the Output Voltage.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See Compensation Components.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100kΩ resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

ABSOLUTE MAXIMUM RATINGS

V_{IN}, Supply Voltage	-0.3V ~ 20V
V_{SW}, Switch Voltage	-1V ~ V_{IN} +0.3V
V_{BS}, Bootstrap Voltage	V_{SW}-0.3V ~ V_{SW} +6V
V_{EN}, Enable/UVLO Voltage	-0.3V ~ +6V
V_{COMP}, Comp Voltage	-0.3V ~ +6V
V_{FB}, Feedback Voltage	-0.3V ~ +6V
Junction Temperature	+150℃
Lead Temperature (Soldering, 10s)	+260℃
Storage Temperature	-65°C ~ +150℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
V_{IN}, Input Voltage	4.75 to 18	V
V_{OUT}, Output Voltage	0.925 to 15	V
Operating Temperature	-40 to +85	℃

NOTE: The device is not guaranteed to function outside of its operating conditions.

THERMAL RESISTANCE

Package	θ_{JA}	θ_{JC}
PSOP8	50℃/W	10℃/W

NOTE: Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Shutdown Supply Current	V_{EN} ≤ 0.3V	-	0.3	3	μA
Supply Current	V_{EN} = 2.0V, V_{FB} = 1.0V	-	1.3	1.5	mA
Feedback Voltage	4.75V≤V_{IN}≤18V	900	925	946	mV
Feedback Overvoltage Threshold		-	1.1	-	V
Error Amplifier Voltage		-	480	-	V/V
Error Amplifier Transconductance	ΔI_C = ±10μA	-	800	-	μA/V
High-Side Switch-On Resistance		-	100	-	mΩ
Low-Side Switch-On Resistance		-	100	-	mΩ
High-Side Switch Leakage	V_{EN} = 0V, V_{SW} = 0V	-	0	10	μA
Upper Switch Current Limit		4	6	-	A
Lower Switch Current Limit		-	0.9	-	A
COMP to Current Sense Transconductance		-	5.2	-	A/V
Oscillator Frequency		310	370	390	kHz
Short Circuit Frequency	V_{FB} = 0V	-	150	-	kHz
Maximum Duty Cycle	V_{FB} = 1.0V	-	90	-	%
Minimum On Time		-	220	-	nS
EN Shutdown Threshold Voltage	V_{EN} Rising	1.1	1.3	1.5	V
EN Shutdown Threshold Voltage Hysterisis		-	40	-	mV
EN Lockout Threshold Voltage		2.2	2.5	2.7	V
EN Lockout Hysterisis		-	210	-	mV
Input UVLO Threshold Rising	V_{IN} Rising	3.8	4.05	4.4	V
Input UVLO Threshold Hysteresis		-	210	-	mV
Soft-start Current	V_{SS} = 0V	-	6	-	μA
Soft-start Period	C_{SS} = 0.1μF	-	15	-	ms
Thermal Shutdown		-	160	-	°C

APPLICATION CIRCUIT

Figure 1. Typical Application Circuit

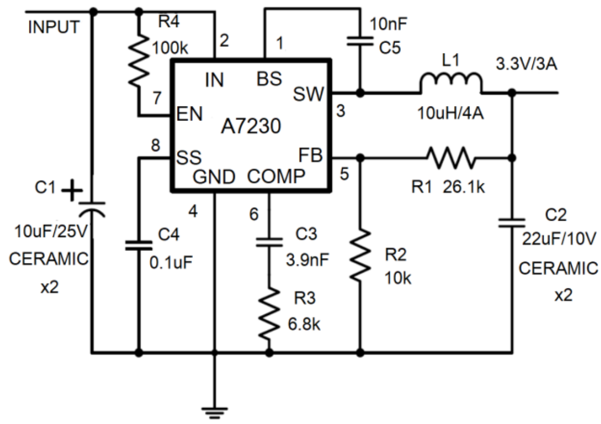
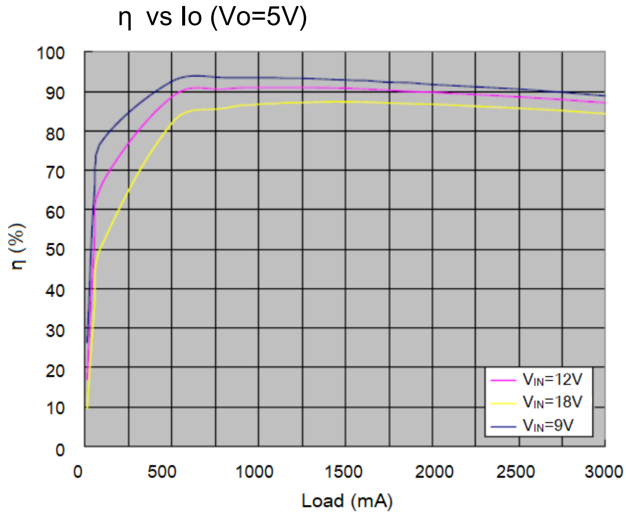
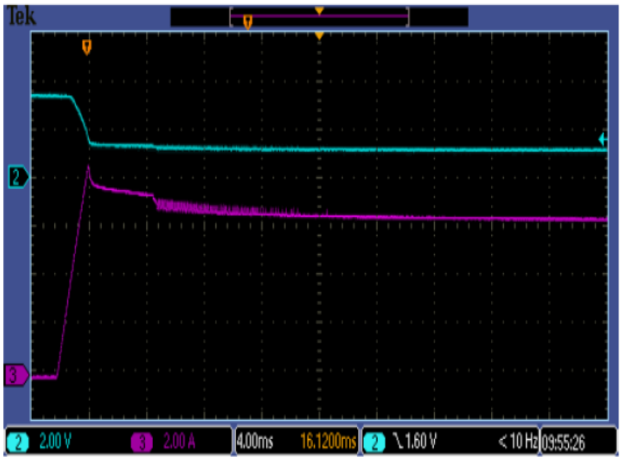


Figure 2. Typical Efficiency Curve



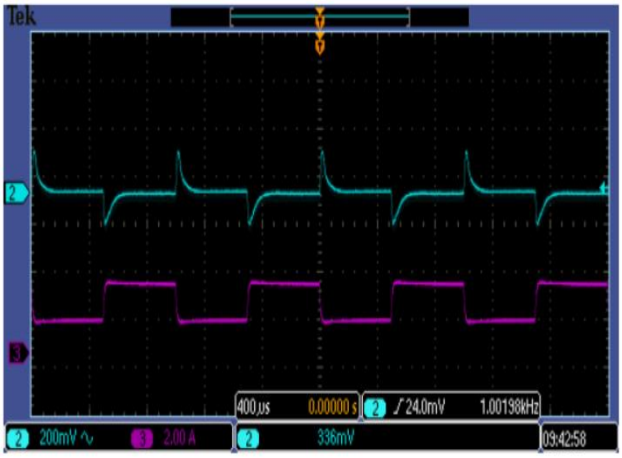
TYPICAL PERFORMENCE CHARACTERISTICS

1. Short circuit test (Channel3:ISW, Channel2:V_O)

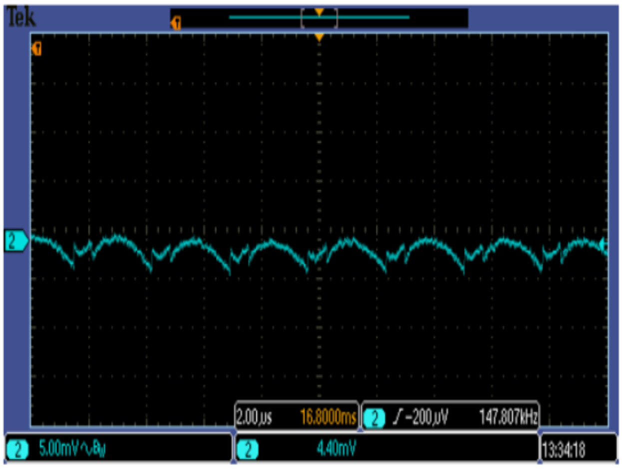


2. Soft-start (Channel1:EN, Channel2:V_O)

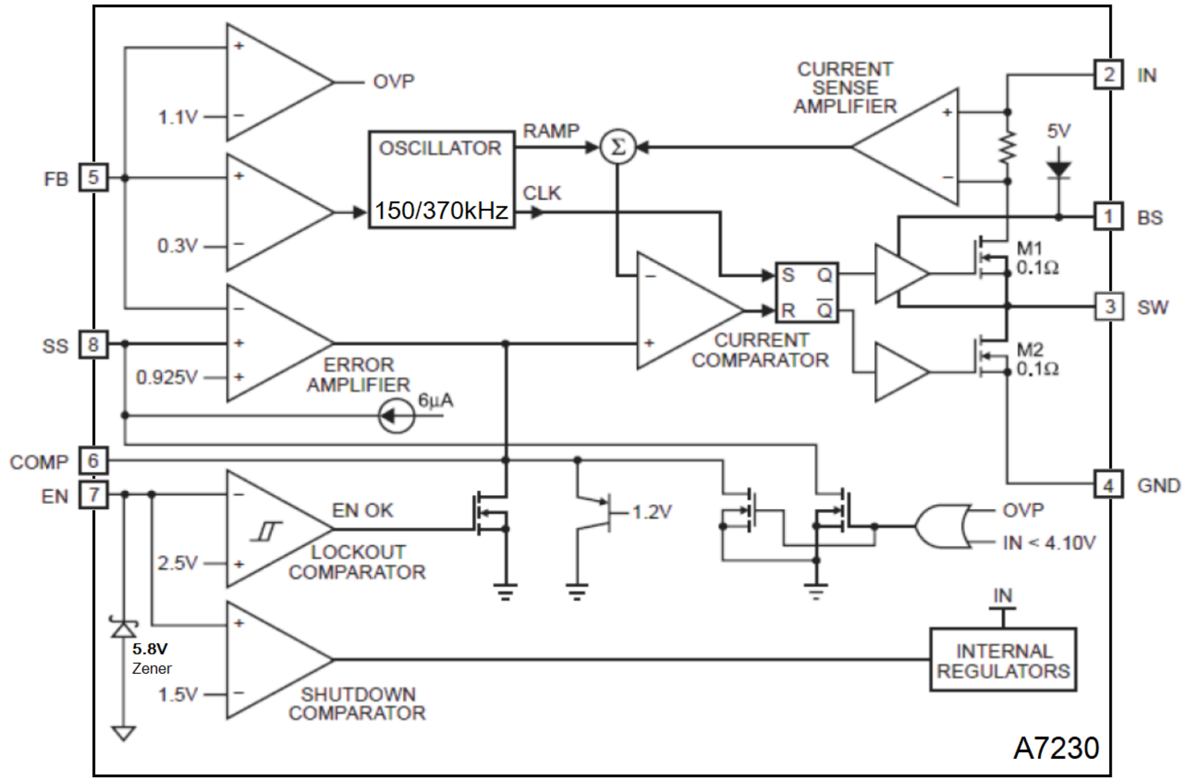
3. Transient response (Channel3:ISW, Channel2:V_O)



4. Ripple



BLOCK DIAGRAM



DETAILED INMFORMATION

The A7230 is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 18V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The A7230 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the A7230 FB pin exceeds 20% of the nominal regulation voltage of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

Component Selection Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB (see Typical Application circuit on page 1). The voltage divider divides the output voltage down by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.
Thus the output voltage is:

$$V_{OUT} = 0.925 \times \frac{R1+R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

$$R1 = 10.81 \times (V_{OUT} - 0.925) \quad (k\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ. Table 1 lists recommended resistance values of R1 and R2 for standard output voltages.

Table.1 Recommended Resistance Values

V_{OUT}	R1	R2
1.8V	9.53kΩ	10kΩ
2.5V	16.9kΩ	10kΩ
3.3V	26.1kΩ	10kΩ
5V	44.2kΩ	10kΩ
12V	121kΩ	10kΩ

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to- peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirements.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes.

Table.2 Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
SM140A	40V, 1A	AiT Semi
MBR130	30V, 1A	AiT Semi

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where ICIN = ILOAD/2. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_s} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} \times \frac{1}{8 \times f_s \times C2}\right)$$

Where C2 is the output capacitance value and RESR is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The A7230 can be optimized for a wide range of capacitance and ESR values. For A7230 normal operation, the output can be an electrolytic capacitor in parallel.

Compensation Components

A7230 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage, 0.925V; AVEA is the error amplifier voltage gain; GCS is the current sense transconductance and RLOAD is the load resistor value. The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where GEA is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6, an additional capacitor from COMP to GND) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good rule of thumb is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_S}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where fc is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, fZ1, below one-forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole fP3 at the location of the ESR zero. Determine the C6 value by the equation:

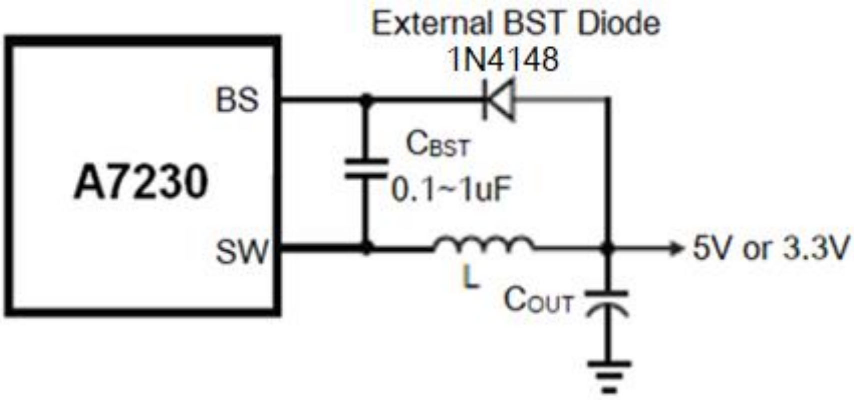
$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BS diode are:

- V_{OUT} is 5V or 3.3V
- Duty cycle is high: $D=V_{OUT}/V_{IN}$ > 65%

In these cases, an external BS diode is recommended from the output of the voltage regulator to BS pin, see below:



Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BS diode is 1N4148, and the BS cap is 0.1~1μF.

The EN pin peripheral components

If it is the just requirement to automatically turn on or off A7230, add 100k resistor between V_{IN} and EN as shown in Figure 3. The internal 5.8V Zener diode on the EN PIN clamps EN pin voltage to 5.8V.

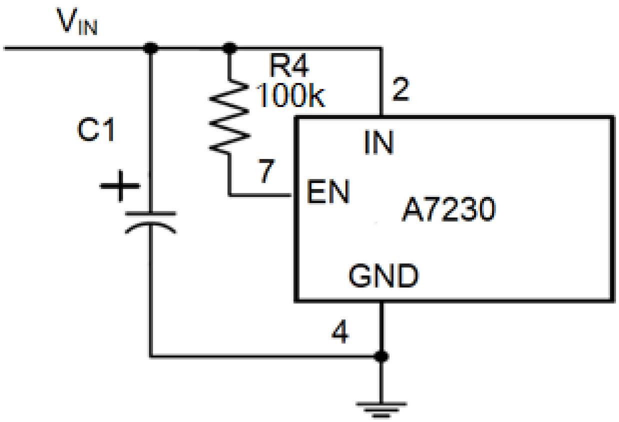


Figure 3 Switch on/off automatically

To enable A7230 by MCU I/O 5V or 3.3V Logic signal, 1k resistor connected between MCU I/O port and the A7230 EN pin is suggested, as shown in figure 4.

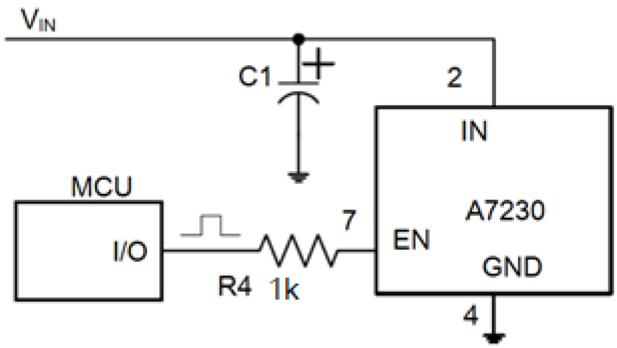


Figure 4 Control by external MCU

To enable A7230 through the mechanical slide switch. In order to prevent the effect of the jitter or spike caused by the switch, a 39k resistor and 0.1uF capacitor together composing a low-pass filter is required, and the time constant of the low-pass filter is approximately 4ms ensure the EN pin not to be disturbed, as shown in Figure 5.

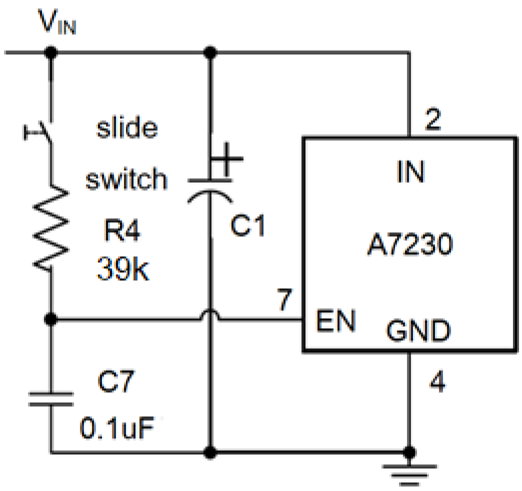
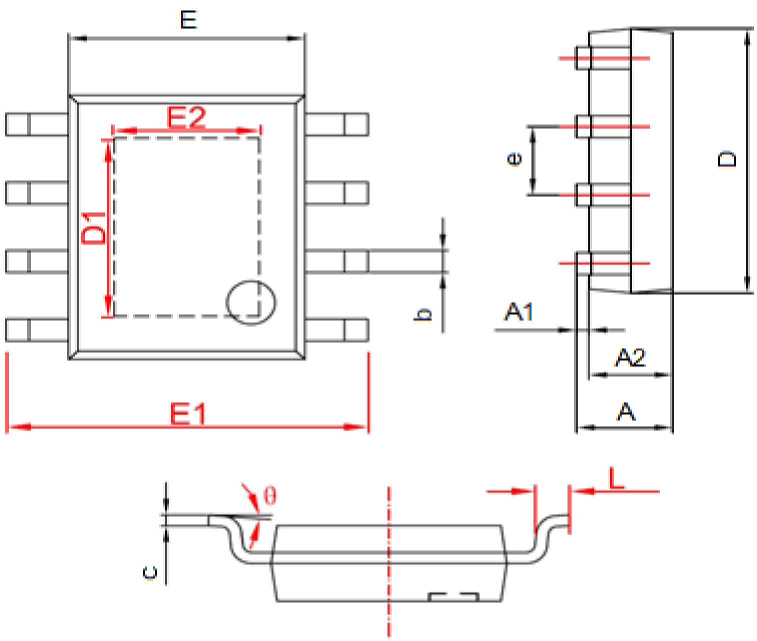


Figure 5 Control by Mechanical sliding switch

PACKAGE INFORMATION

Dimension in PSOP8 Package (Unit: mm)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

IMPORTANT NOTICE