DESCRIPTION

The A7112 is a high-efficiency, DC-to-DC step-down switching regulators, capable of delivering up to 1.2A of output current. The device operates from an input voltage range of 2.6V to 7V and provides an output voltage from 0.6V to V_{IN}, making the A7112 ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. This low noise output along with its excellent efficiency achieved by the internal synchronous rectifier, making A7112 an ideal green replacement for large power consuming linear regulators. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

The A7112 is available in SOT-25 and DFN6(2x2) packages.

ORDER INFORMATION

Package Type	Part Number	
SOT-25	E5	A7112E5R-ADJZ
		A7112E5VR-ADJZ
DFN6(2x2)	J6	A7112J6R
		A7112J6VR
Note	Z: Pin Type V: Halogen free Package R: Tape & Reel SPQ: 3k/Reel	
AiT provides all RoHS products Suffix “V” means Halogen free Package		

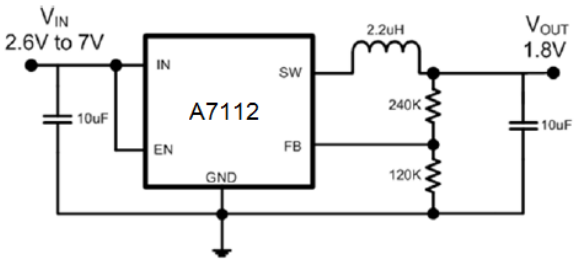
FEATURES

- High Efficiency: Up to 97%
- Capable of Delivering 1.2A
- 1.5MHz Switching Frequency
- No External Schottky Diode Needed
- Low dropout 100% Duty operation
- Internal Compensation and Soft-Start
- Current Mode control
- 0.6V Reference for Low Output voltages
- Logic Control Shutdown (I_Q<1uA)
- Thermal shutdown, UVLO
- Available in SOT-25 and DFN6(2x2)packages

APPLICATION

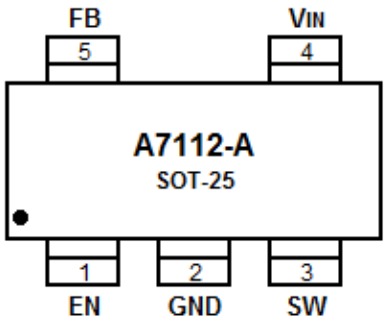
- Cellular phones
- Digital Cameras
- MP3 and MP4 players
- Set top boxes
- Wireless and DSL Modems
- USB supplied Devices in Notebooks
- Portable Devices

TYPICAL APPLICATION

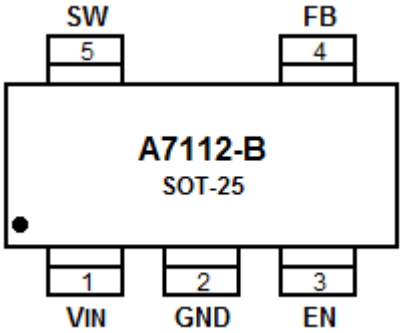


1.8V Step-Down Converter

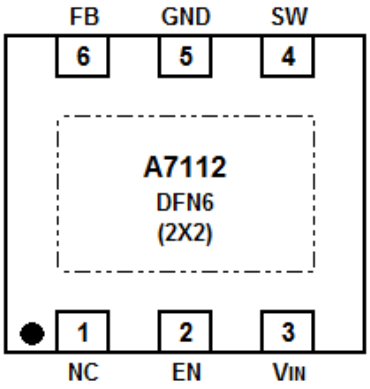
PIN DESCRIPTION



Top View



Top View



Top View

Pin #			Symbol	Function
SOT-25A	SOT-25B	DFN6 (2x2)		
1	3	2	EN	Enable pin for the IC. Drive the pin to high to enable the part, and low to disable
2	2	5	GND	Ground
3	5	4	SW	Inductor connection. Connect an inductor between SW and the regulator output.
4	1	3	V_{IN}	Supply voltage.
5	4	6	FB	Feedback input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and V_{IN}
-	-	1	NC	Not connected

ABSOLUTE MAXIMUM RATINGS

Max Input Voltage		8V
T_J ,Max Operating Junction Temperature		125℃
T_A, Ambient Temperature		-40℃~85℃
Maximum Power Dissipation	SOT-25	400mW
	DFN6(2x2)	600mW
Ts, Storage Temperature		-40℃~150℃
Lead Temperature & Time		260℃, 10s
HBM,ESD		>2000V

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value
Input Voltage Range		7V
Operating Junction Temperature	T_J	-20℃~125℃

ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_A=25℃

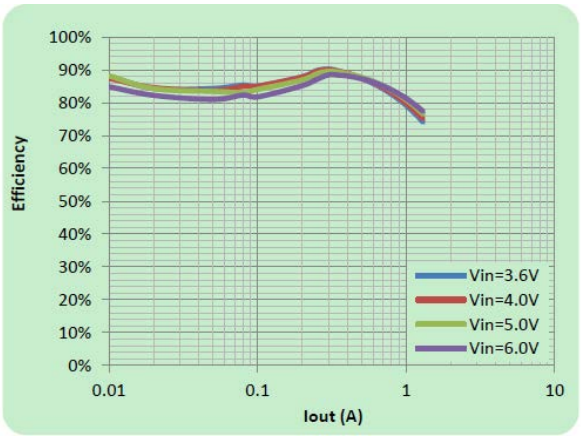
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		7	V
Feedback Voltage	V_{REF}	V_{IN}=5V	0.588	0.6	0.612	V
Feedback Leakage Current	I_{FB}			0.1	1	uA
Quiescent Current	I_Q	Active, V_{FB}=0.65, No Switching		50		uA
		Shutdown			1	
Line Regulation	LnReg	V_{IN}=2.7V to 5.5V		0.1	0.2	%/V
Load Regulation	LdReg	I_{OUT}=0.01 to 1A		0.1	0.2	%/A
Switching Frequency	F_{SOC}		1.1	1.5	1.9	MHz
PMOS R_{DSON}	$R_{DSON}P$			250	350	mΩ
NMOS R_{DSON}	$R_{DSON}N$			150	250	mΩ
Peak Current Limit	I_{LIMIT}		1.2	1.5	2	A
	Inoload*	V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0		75		uA
SW Leakage Current	I_{SWLK}	V_{OUT}=6V, V_{SW}=0 or 6V, EN=0V			1	uA
EN Leakage Current	I_{ENLK}				1	uA
EN Input High Voltage	V_{H_EN}		1			V
EN Input Low Voltage	V_{L_EN}				0.5	V

NOTE: *When Dutycycle >80%, Inoload will increase. e.g. V_{IN}=3.6V/V_{OUT}=3.3V, Inoload=1mA.

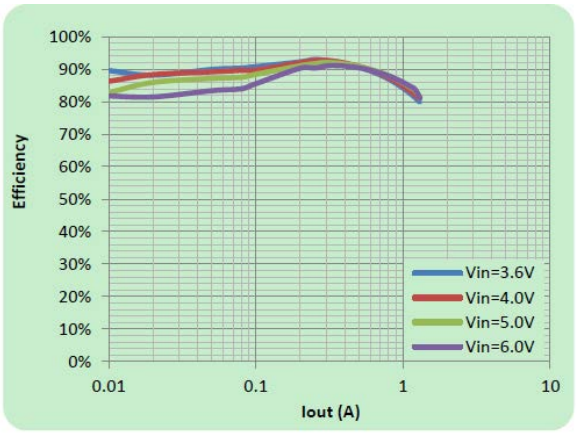
TYPICAL PERFORMANCE CHARACTERISTICS

Tested under T_A=25°C, unless otherwise specified

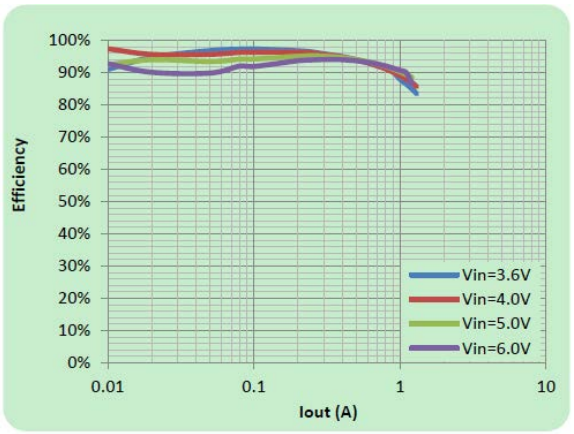
1. Efficiency vs. Output Current, V_{OUT}= 1.2V



2. Efficiency vs. Output Current, V_{OUT}= 1.8V

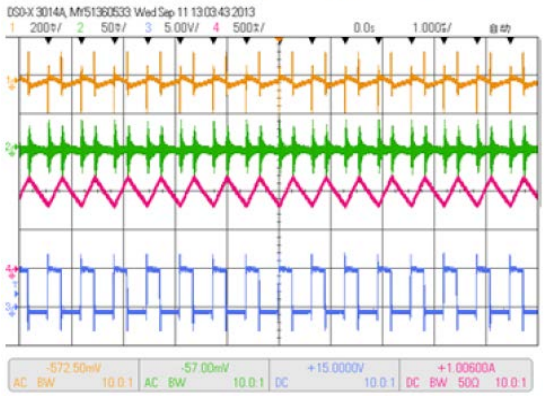


3. Efficiency vs. Output Current, V_{OUT}= 3.3V

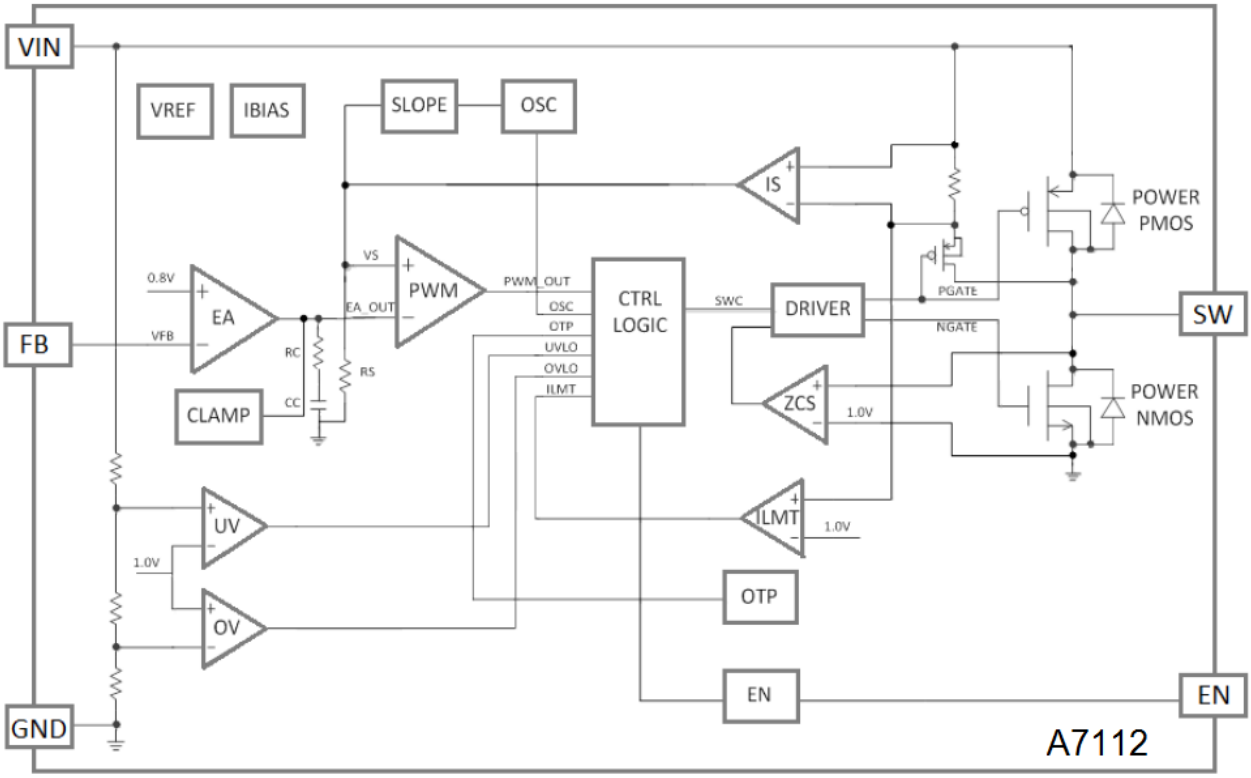


4. Output Ripple and SW at 1A load,
V_{IN}=5V / V_{OUT}=1.8V

Ch1—Vin, Ch2—Vout, Ch3—Vsw



BLOCK DIAGRAM



DETAILED INFORAMTION

The A7112 high-efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 1A of output current. The device operates in pulse-width modulation (PWM) at 1.5MHz from a 2.6V to 7V input voltage and provides an output voltage from 0.6V to V_{IN}, making the A7112 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Loop Operation

A7112 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET of 1.5A (typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. A7112 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to 1.5A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

A7112 has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If V_{IN} drops below 2.5V, the UVLO circuit inhibits switching. Once V_{IN} rises above 2.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Design Procedure

Setting Output Voltages

Output voltages are set by external resistors. The FB_ threshold is 0.6V.

$$R_{TOP} = R_{BOTTOM}[(V_{OUT} / 0.6) - 1]$$

Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$$V_{RIPPLE} = I_{L(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$$V_{RIPPLE(ESR)} = I_{L(PEAK)} \times ESR$$

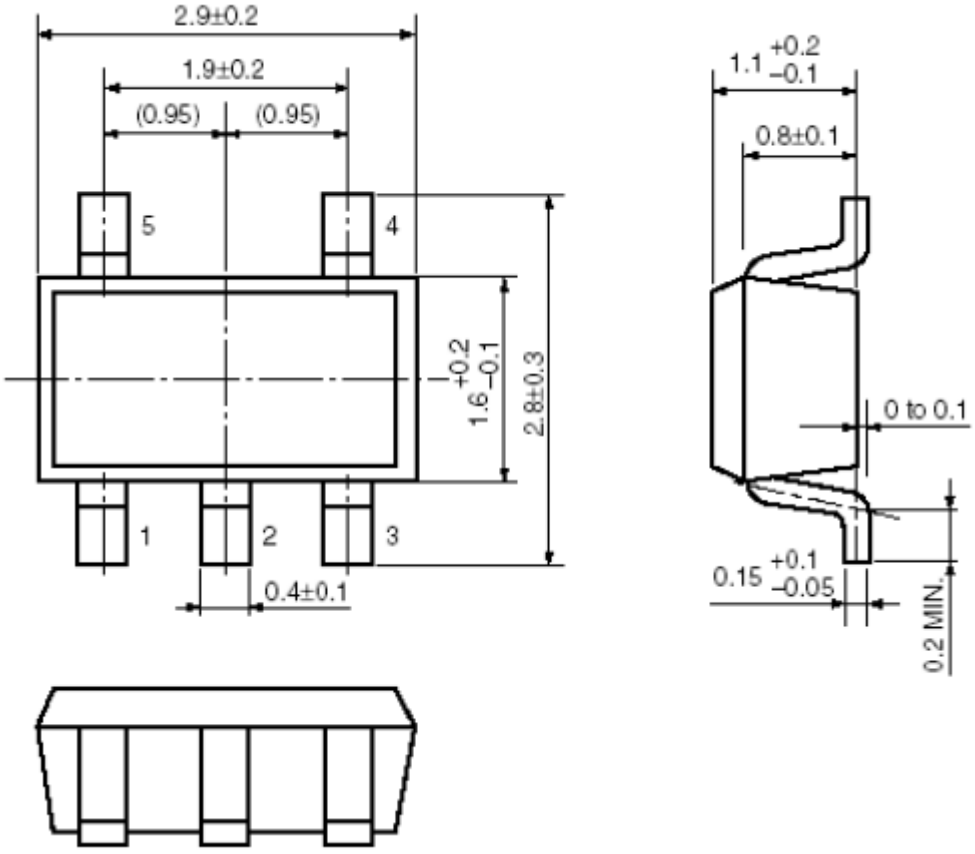
Application Information

Layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

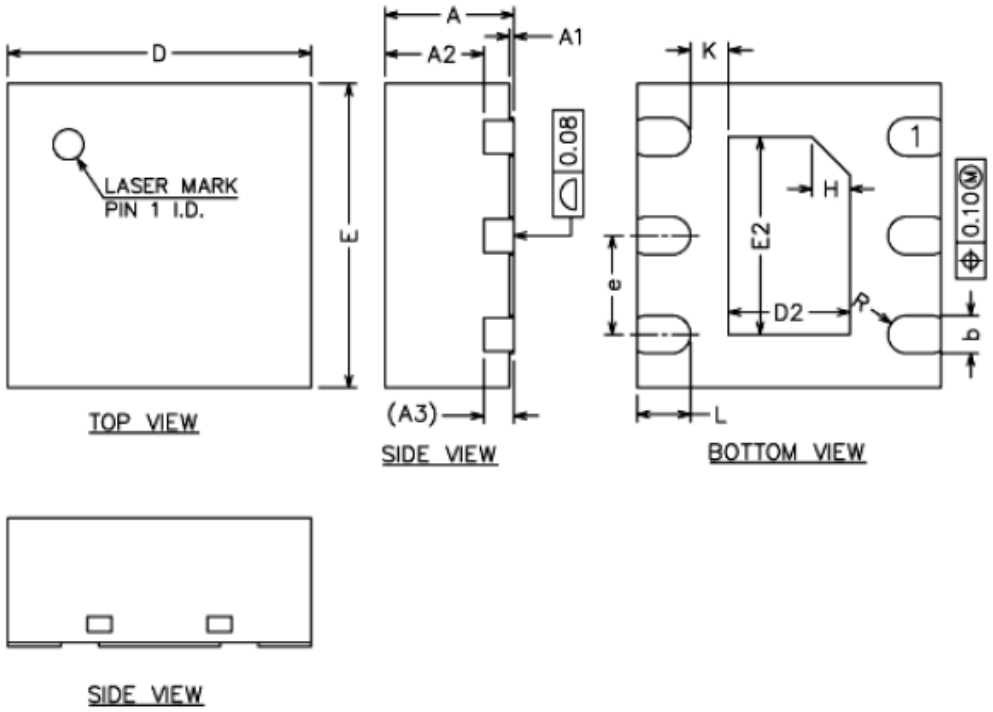
1. Place decoupling capacitors as close to the IC as possible
2. Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.
3. Keep the high-current paths as short and wide as possible. Keep the path of switching current (C1 to V_{IN} and C1 to GND) short. Avoid vias in the switching paths.
4. If possible, connect V_{IN}, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5. Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6. Route high-speed switching nodes away from sensitive analog areas

PACKAGE INFORMATION

Dimension in SOT-25 (Unit: mm)



Dimension in DFN6(2x2) (Unit: mm)



Symbol	Min	Max
A	0.80	0.90
A1	0.00	0.05
A2	0.60	0.70
A3	0.20REF.	
b	0.18	0.30
D	1.90	2.10
E	1.90	2.10
D2	0.70	0.90
E2	1.20	1.40
e	0.55	0.75
H	0.25REF.	
K	0.20	-
L	0.30	0.40
R	0.11	-

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