DESCRIPTION

The A6318 is a high performance linear voltage regulator with adjustable output with a 1.23 reference voltage. It operates from an input of 2V to 6V and provides output current up to 300mA with two external resistors to set the output voltage. The A6318 designed for portable RF and wireless applications with demanding performance and space requirements. Optimized for battery-powered systems to deliver ultra-low noise and low quiescent current. A noise FB pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

The A6318 works with low-ESR ceramic capacitors, reducing the PCB space. The A6318 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs.

The A6318 has superior regulation over variations in line and load. Also it provides fast respond to step changes in load. Other features include over-current and over-temperature protection and high ripple rejection ratio.

The A6318 is available in SOT-25 package

ORDERING INFORMATION

Package Type	Part Number	
SOT-25 SPQ: 3,000pcs/Reel	E5	A6318E5R-ADJ
		A6318E5VR-ADJ
Note	ADJ=Adjustable V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

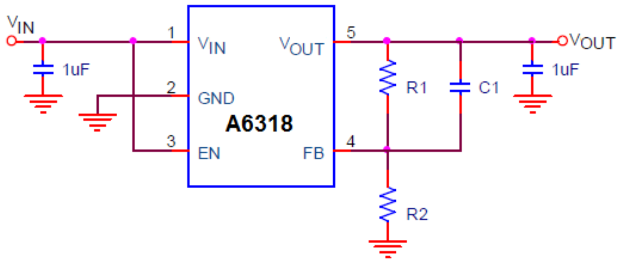
FEATURES

- Low Dropout:210mV@300mA
- TTL-logic-Controlled Shutdown Input
- <0.01μA Standby Current When Shutdown
- Ultra-low noise for RF Application
- Ultra-Fast Response in Line/Load Transient
- Quick Start-Up (Typically 50μS)
- Wide Operating Voltage Ranges: 2V to 6V
- Low Temperature Coefficient
- Current Limiting Protection
- Thermal Shutdown Protection
- Only 1μF Output Capacitor Required for Stability
- High Power Supply Rejection Ratio
- Fast output discharge
- Available in SOT-25 package

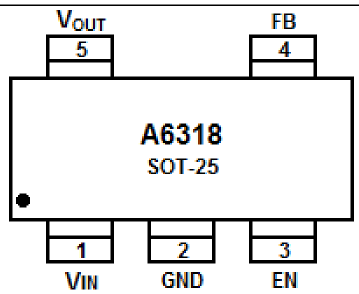
APPLICATION

- Battery-Powered Equipment
- Cellular and Smart Phones
- Graphic Card, Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- Peripheral Cards
- PCMCIA Card

TYPICAL APPLICATION



PIN DESCTRIPTION



Top View

Pin #	Symbol	Function
1	V_{IN}	Power Input Voltage
2	GND	Ground
3	EN	Active high with internal 8 mΩ pull down
4	FB	Feedback
5	V_{OUT}	Output Voltage

ABSOLUTE MAXIMUM RATING

V_{CC}, Input Supply Voltage	-0.3V ~ +6V
EN Input Voltage	-0.3V ~ +V_{IN}
Output Voltage	-0.3V ~ V_{IN}+0.3V
FB Voltage	-0.3V ~ V_{IN}+0.3V
Output Current	300mA
P_D, Power Dissipation	350mW
Maximum Junction Temperature	125°C
Operating Temperature Range[NOTE1]	-40°C ~ 85°C
Storage Temperature Range	-65°C ~ 125°C
Lead Temperature (Soldering, 10s)	300°C

Stresses beyond may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE1: The A6318 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

THERMAL RESISTANCE[NOTE2]

Package	θ_{JA}	θ_{JC}
SOT-25	250°C/W	130°C/W

NOTE2: Thermal Resistance is specified with approximately 1 square of 1 oz copper

ELECTRICAL CHARACTERISTICS[NOTE3]

V_{IN}=3.6V, EN=V_{IN}, C_{IN}=C_{OUT}=1μF, C_{FB}=22nF, T_A=25℃, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input Voltage	V_{IN}		2	-	6	V
Output Voltage Accuracy	ΔV_{OUT}	V_{IN}=3.6V, I_{OUT}=1mA	-1	-	+1	%
			-2	-	+2	
		V_{IN}=3.4V, I_{OUT}=300mA	-2.5	-	+2.5	
Current Limit	I_{LIM}	R_{LOAD}=1Ω	400	430	-	mA
Quiescent Current	I_Q	V_{EN}>1.2V, I_{OUT}=0mA	-	90	130	μA
Dropout Voltage	V_{DROP}	I_{OUT}=200mA, V_{OUT}=2.8V	-	130	180	mV
		I_{OUT}=300mA, V_{OUT}=2.8V	-	210	300	
Line Regulation[NOTE4]	ΔV_{LINE}	V_{IN}=3.6V to 5.5V, I_{OUT}=1mA	-	0.05	0.17	%/V
Load Regulation[NOTE5]	ΔV_{LOAD}	1mA<I_{OUT}<300mA	-	-	2	%/A
Output Voltage Temperature Coefficient[NOTE6]	TC_{VOUT}	I_{OUT}=1mA	-	±60	-	ppm/℃
Standby Current	I_{STBY}	V_{EN}=GND, Shutdown	-	0.01	1	μA
EN Input Bias Current	I_{IBSD}	V_{EN}=GND or V_{IN}	-	0	100	nA
EN Input Threshold — Logic Low	V_{IL}	V_{IN}=3V to 5.5V,Shutdown	-	-	0.4	V
EN Input Threshold — Logic High	V_{IH}	V_{IN}=3V to 5.5V,Start up	1.2	-	-	
Output Noise Voltage	e_{NO}	10Hz to100kHz, I_{OUT}=200mA, C_{OUT}=1μF	-	100	-	$μV_{RMS}$
Power Supply Rejection Ratio — f=217Hz	PSRR	C_{OUT}=1uF, I_{OUT}=100mA	-	-80	-	dB
Power Supply Rejection Ratio — f=1kHz			-	-78	-	
Power Supply Rejection Ratio — f=10kHz			-	-65	-	
Thermal Shutdown Temperature	T_{SD}	Shutdown, Temp increasing	-	165	-	℃
Thermal Shutdown Hysteresis	T_{SDHY}		-	30	-	℃

NOTE3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

NOTE4: Line regulation is calculated by ΔV_{LINE}= $[(V_{OUT1}-V_{OUT2})/(\Delta V_{IN} x V_{OUT(normal)})]x100$

Where V_{OUT1} is the output voltage when V_{IN}=5.5V, and V_{OUT2} is the output voltage when V_{IN}=3.6V, ΔV_{IN}=1.9V .$V_{OUT(normal)}$=2.8V

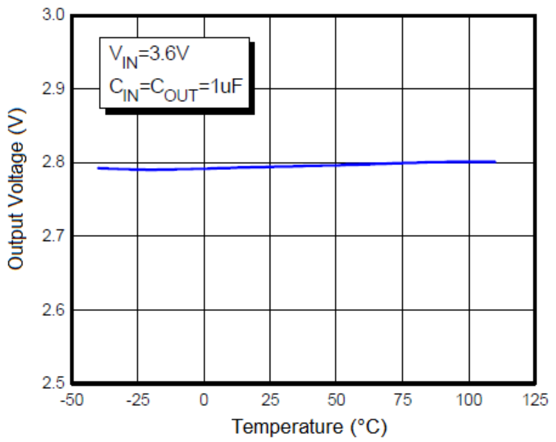
NOTE5: Load regulation is calculated by ΔV_{LOAD}= $[(V_{OUT1}-V_{OUT2})/(\Delta I_{OUT} x V_{OUT(normal)})]x100$

Where V_{OUT1} is the output voltage when I_{OUT}=1mA, and V_{OUT2} is the output voltage when I_{OUT}=300mA. ΔI_{OUT}=0.299A, $V_{OUT\ (normal)}$ =2.8V.

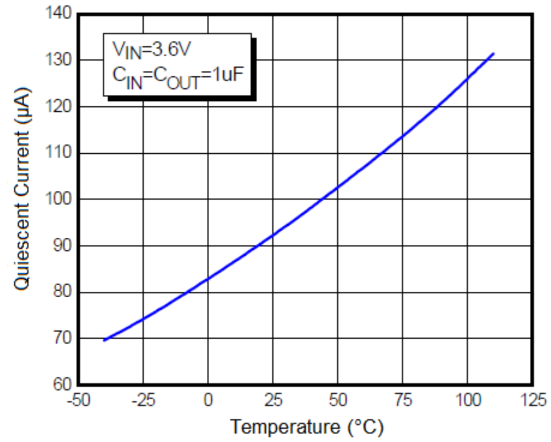
NOTE6: The temperature coefficient is calculated by $TC_{VOUT}=\Delta V_{OUT} /(\Delta T x V_{OUT})$

TYPICAL PERFORMANCE CHARACTERISTICS

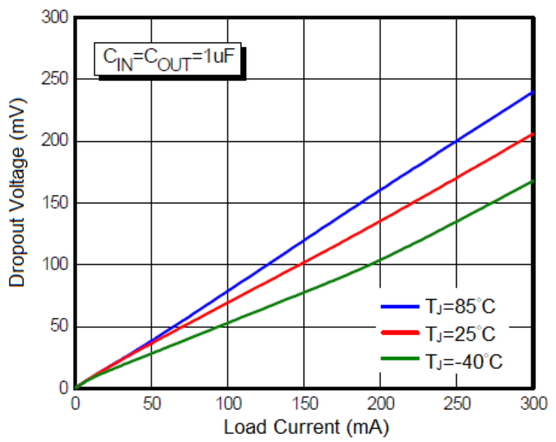
1. Output Voltage vs. Temperature



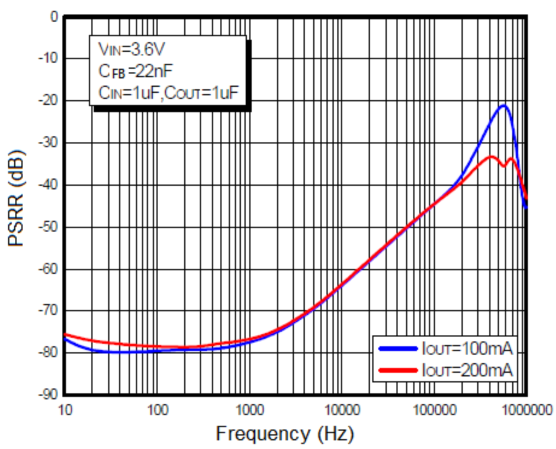
2. Quiescent Current vs. Temperature



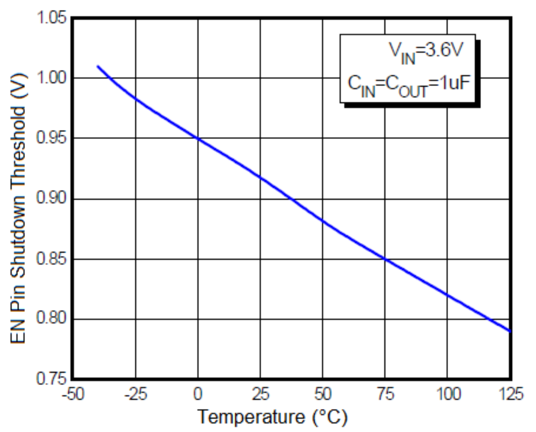
3. Dropout Voltage vs. Load Current



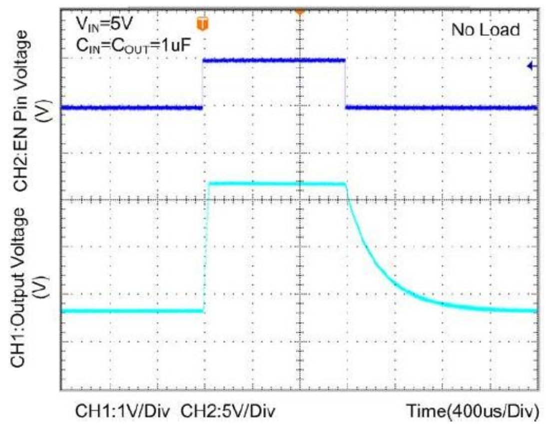
4. PSRR



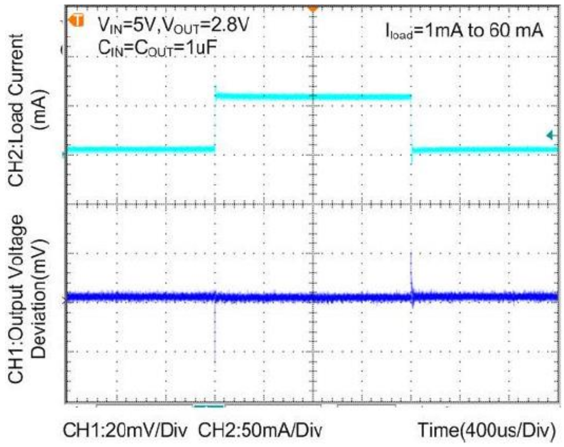
5. EN Pin Shutdown Threshold vs. Temperature



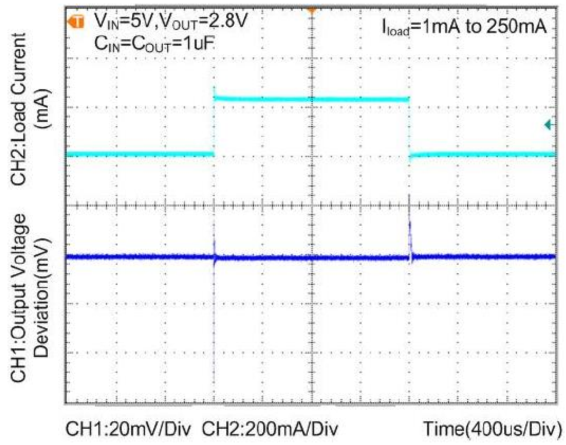
6. EN Pin Shutdown Response



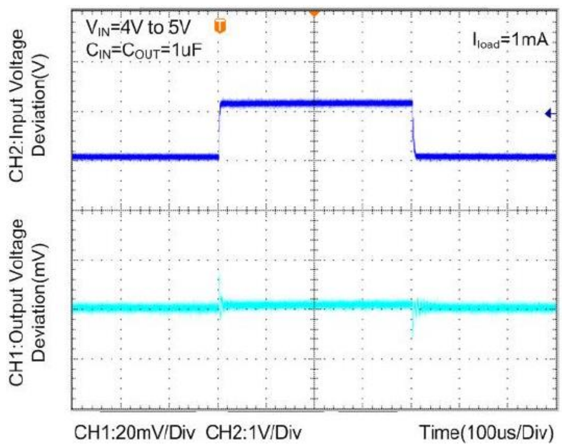
7. Load Transient Response



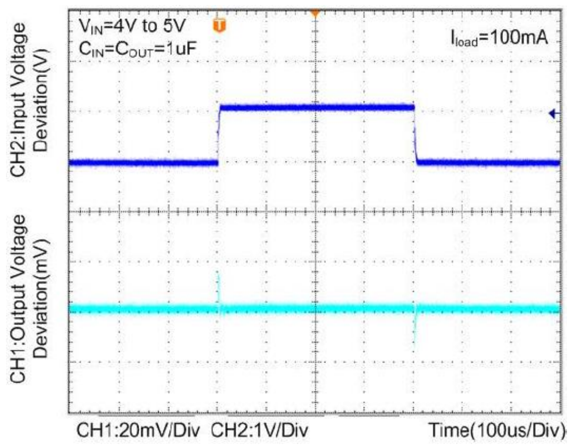
8. Load Transient Response



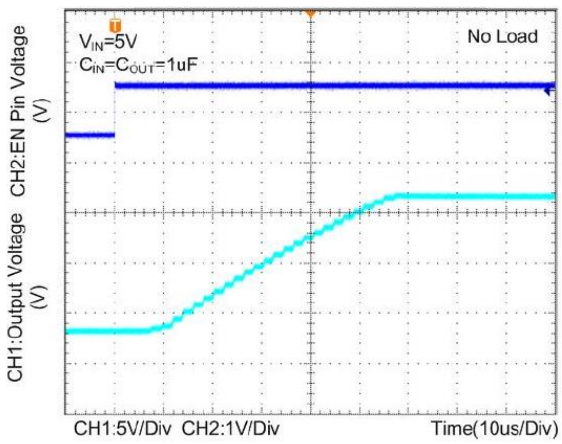
9. Line Transient Response



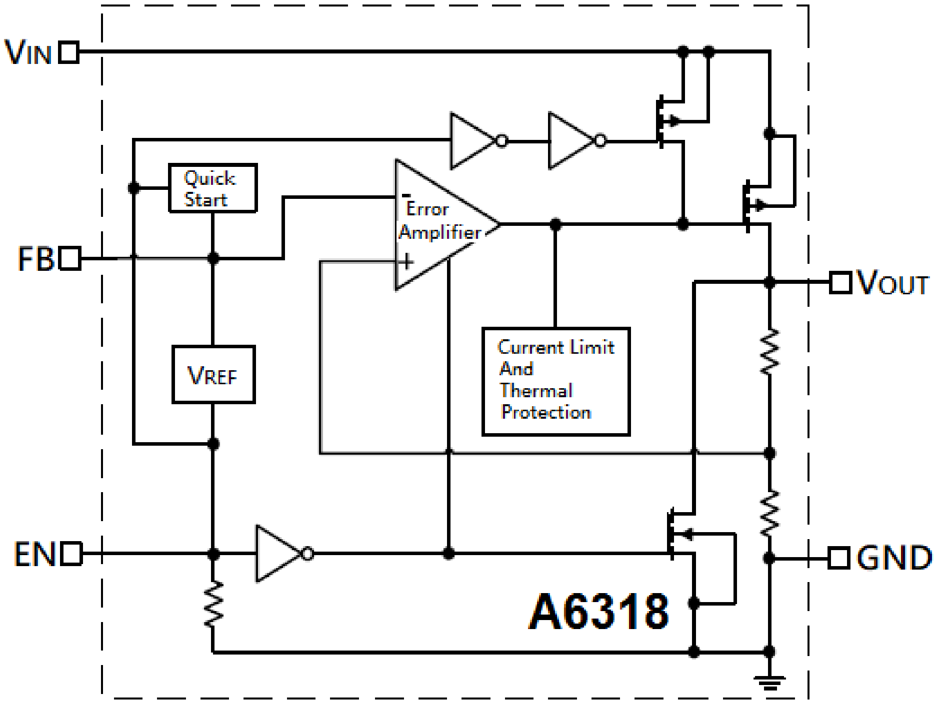
10. Line Transient Response



11. Start Up



BLOCK DIAGRAM



APPLICATIONS INFORMATION

Like any low-dropout regulator, the external capacitors used with the A6318 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the A6318 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground.

Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application.

The A6318 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the A6318 output ensures stability. The A6318 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the A6318 and returned to a clean analog ground.

FB Capacitor and Low Noise

Connecting a 22nF between the FB pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the FB pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the FB capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

Enable Function

The A6318 features an LDO regulator enable/ disable function. To assure the LDO regulator will switch on; the EN turn on control level must be greater than 1.2 volts.

The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protect the system, the A6318 have a quick discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Programming the A6318 Adjustable LDO regulator

The output voltage of the A6318 adjustable regulator is programmed using an external resistor divider as show in Figure as below. The output voltage is calculated using equation as below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where: V_{REF}=1.23V typ. (the internal reference voltage) .Resistors R1 and R2 should be chosen for approximately 50uA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decrease/increases V_{OUT}. The recommended design procedure is to choose R2=30.1kΩ to set the divider current at 50uA, C1=22pF for stability, and then calculate using Equation as below:

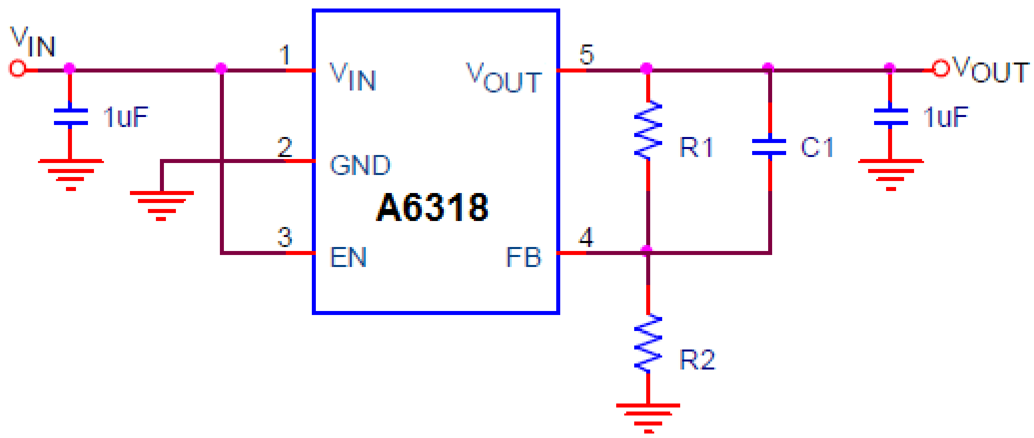
$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. The suggested value of this capacitor for several resistor ratios is shown in the table below.

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGTE	R1	R2	C1
1.8V	13.9 kΩ	30.1 kΩ	22pF
2.5V	31.6 kΩ	30.1 kΩ	22pF
3.3V	51 kΩ	30.1 kΩ	22pF
3.6V	59 kΩ	30.1 kΩ	22pF

A6318 Adjustable LDO regulator Programming



Thermal Considerations

Thermal protection limits power dissipation in A6318. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 30°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$$

Where $T_J(MAX)$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of A6318, where $T_J(MAX)$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT-25 package is 250°C/W, on standard JEDEC 51-3 thermal test board. The maximum power dissipation at T_A= 25°C can be calculated by following formula:

$$P_D(MAX) = (125°C - 25°C)/250 = 400mW$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_J(MAX)$ and thermal resistance θ_{JA}. It is also useful to calculate the junction of temperature of the A6318 under a set of specific conditions. In this example let the Input voltage V_{IN}=3.3V, the output current Io=300mA and the case temperature T_A=40°C measured by a thermal couple during operation. The power dissipation for the V_{OUT}=2.8V version of the A6318 can be calculated as:

$$P_D = (3.3V - 2.8V) \times 300mA + 3.6V \times 100uA = 150mW$$

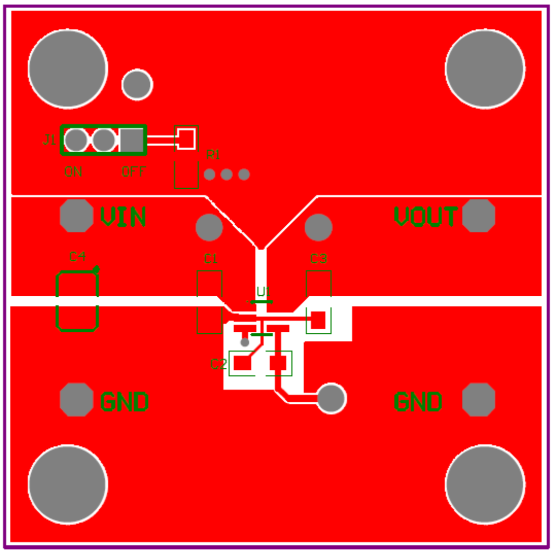
And the junction temperature, T_J, can be calculated as follows:

$$T_J = T_A + P_D \times \theta_{JA} = 40°C + 0.15W \times 250°C/W = 40°C + 37.5°C = 77.5°C < T_J(MAX) = 125°C$$

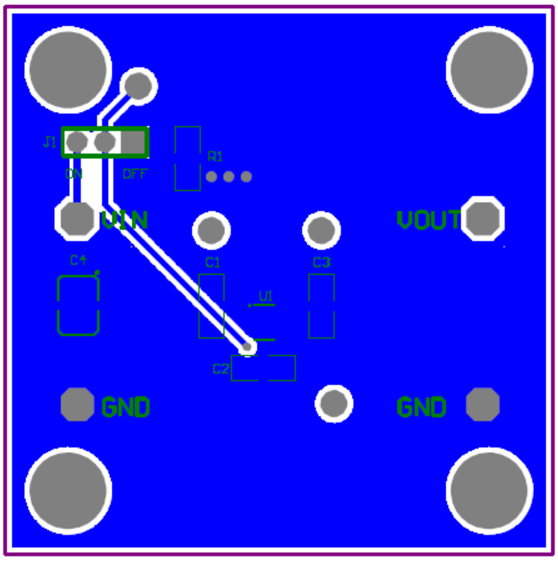
For this operating condition, T_J is lower than the absolute maximum operating junction temperature, 125°C, so it is safe to use the A6318 in this configuration.

Layout considerations

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the FB capacitor should connect directly to the GND pin of the device.



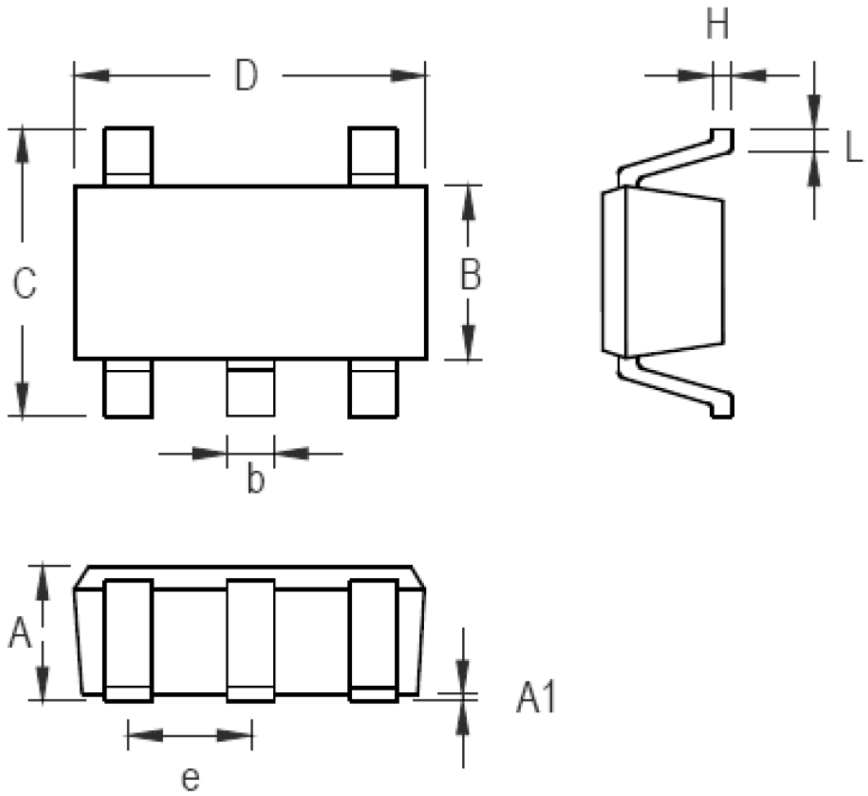
TOP Layer Layout



BOTTOM Layer Layout

PACKAGE INFORMATION

Dimension in SOT-25 (Unit: mm)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

IMPORTANT NOTICE

AiT Semiconductor Inc. (AiT) reserves the right to make changes to any its product, specifications, to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

AiT Semiconductor Inc.'s integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life support applications, devices or systems or other critical applications. Use of AiT products in such applications is understood to be fully at the risk of the customer. As used herein may involve potential risks of death, personal injury, or server property, or environmental damage. In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

AiT Semiconductor Inc. assumes to no liability to customer product design or application support. AiT warrants the performance of its products of the specifications applicable at the time of sale.