DESCRIPTION

The A2323 is TDD suppression, super low EMI, single channel, class-D audio power amplifier.

The A2323 designed with the dedicated EEE (Enhanced Emission Elimination) technology, reducing great EMI jamming in full frequency span range, relative to 60cm audio cable, with more than 20dB level capability in FCC standard.

The A2323 internal professional timing control circuit, fully Suppressed the “Pop-Click” sound, can effectively erase the transient noise during power up, power down, power weak and power off in system operation.

The A2323 internal over current protection function and thermal protection function, can effectively protected chip operation form abnormal damage condition.

The A2323 is available in FC-9 package.

ORDERING INFORMATION

Package Type	Part Number	
FC-9	F9	A2323F9R
		A2323F9VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products Suffix “ V “ means Halogen free Package		

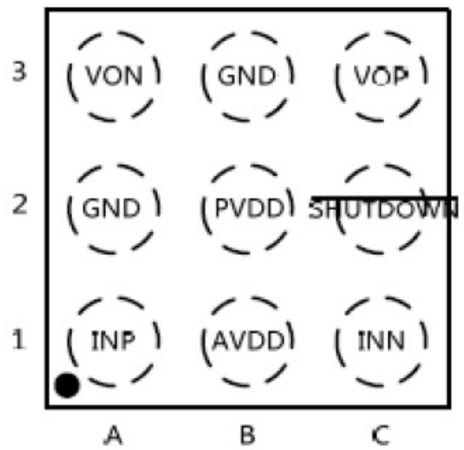
FEATURES

- Dedicated RNS(RF-TDD Noise Suppression) technology
- The EEE technology is a super reduction capability in full frequency span EMI suppression.
- Excellent in the “Pop-Click” noise suppression.
- High PSRR: -70 dB (217Hz).
- Support 1.8V control logic.
- 0.1% THD+N (0.4W output power, 4.2V power).
- 1.15W output power(10% THD ,4.2V power,8Ω load).
- High efficiency in 90%.
- Low quiescent current (2.6mA).
- Low shut down current (<0.1uA).
- Over current protection, hyper thermal protection.
- ESD discharged protection : ±8kV (HBM).
- Latch-up : ± 450 mA.
- Available in FC-9 Package

APPLICATION

- Mobile phone
- PDA, GPS, MP3
- Portable electronic devices

PIN DESCRIPTION



Top View

Pin #	Symbol	Function
A1	INP	Positive audio signal input
A2	GND	Ground
A3	VON	Negative audio signal output
B1	AV_{DD}	Simulation power
B2	PV_{DD}	Power source
B3	GND	Ground
C1	INN	Negative audio signal input
C2	$\overline{SHUTDOWN}$	Shut down
C3	VOP	Positive audio signal output

ABSOLUTE MAXIMUM RATING

V_{DD} Supply Voltage	-0.3V~6V
INP , INN Pin Voltage	-0.3V~V_{DD}+0.3V
Θ_{JA}, Package Thermal Resistance	90℃/W
Operating Temperature	-40℃~85℃
T_{JMAX}, Maximum Operating Temperature	125℃
T_{STG}, Storage Temperature	-65℃~150℃
Pin Temperature (Soldering in 10 Sec.)	260℃
ESD Range [Note1]	
HBM(Human Body Model)	±8kV
Latch-Up	
Test Standard: JEDEC STANDARD NO. 78B DECEMBER 2008	+IT : 450mA -IT : -450mA

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. There are stress ratings only and operations of the device at these or any other condition beyond those indicated in the operational section of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE1: HBM testing method is which the 100pF capacitor electron passing discharged to IC lead pin through a 1.5kΩ resistor. Testing standards: MIL-STD-883G Method 3015.7

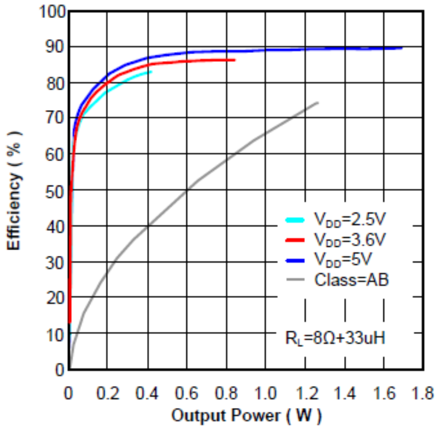
ELECTRICAL CHARACTERISTICS

Test Condition : T_A= 25℃(unless otherwise noted)

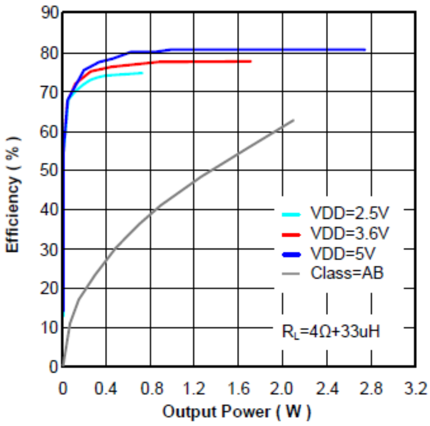
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Electric Characteristic						
Input Voltage Range	V_{DD}		2.5		5.5	V
$\overline{SHUTDOWN}$ High-level input	V_{IH}		1.3		V_{DD}	V
$\overline{SHUTDOWN}$ Low-level input	V_{IL}		0		0.35	V
Output offset voltage	$\|V_{OS}\|$	V_{IN}=0V，A_V=2V/V，V_{DD}=2.5V to 5.5V		5	25	mV
Quiescent Current	I_Q	V_{DD}=3.6V		2.6		mA
Shut down Current	I_{SD}	V_{DD}=3.6V， $\overline{SHUTDOWN}$ =0V		0.1		μA
Power Supply Rejection Ratio	PSRR	217Hz		-70		dB
Common Mode Rejection Ratio	CMRR			-70		dB
Switching frequency	f_{SW}	V_{DD}=2.5V to 5.5V		800		kHz
Amplifier Gain	Gain			$\frac{315\,k\Omega}{R_{IN}}$		V/V
Operation Characteristic						
Output Power	P_O	THD+N=10%,f=1kHz, R_L=4Ω, V_{DD}=5V		2.65		W
		THD+N=1%,f=1kHz, R_L=4Ω, V_{DD}=5V		2.15		
		THD+N=10%,f=1kHz, R_L=8Ω, V_{DD}=5V		1.70		
		THD+N=1%,f=1kHz, R_L=8Ω, V_{DD}=5V		1.35		
		THD+N=10%,f=1kHz, R_L=4Ω, V_{DD}=4.2V		1.85		
		THD+N=1%,f=1kHz, R_L=4Ω, V_{DD}=4.2V		1.50		
		THD+N=10%,f=1kHz, R_L=8Ω, V_{DD}=4.2V		1.15		
		THD+N=1%,f=1kHz, R_L=8Ω, V_{DD}=4.2V		0.90		
		THD+N=10%,f=1kHz, R_L=4Ω, V_{DD}=3.6V		1.35		
		THD+N=1%,f=1kHz, R_L=4Ω, V_{DD}=3.6V		1.05		
		THD+N=10%,f=1kHz, R_L=8Ω, V_{DD}=3.6V		0.85		
		THD+N=1%,f=1kHz, R_L=8Ω, V_{DD}=3.6V		0.65		
Total Harmonic Distortion + Noise	THD+N	V_{DD}=5V, P_O=0.6W, R_L=8Ω, f=1kHz		0.1		%
		V_{DD}=4.2V, P_O=0.4W, R_L=8Ω, f=1kHz		0.1		%
		V_{DD}=3.6V, P_O=0.3W, R_L=8Ω, f=1kHz		0.1		%
Efficiency	η	V_{DD}=5V, P_O=1W, R_L=8Ω, f=1kHz		90		%
Start Time	t_{ST}			40		ms

TYPICAL PERDORMANCE CHARACTERISTICS

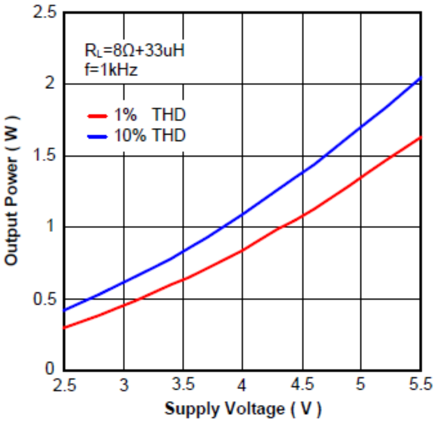
1. EFFICIENCY vs. OUTPUT POWER



2. EFFICIENCY vs. OUTPUT POWER



3. OUTPUT POWER vs. SUPPLY VOLTAGE



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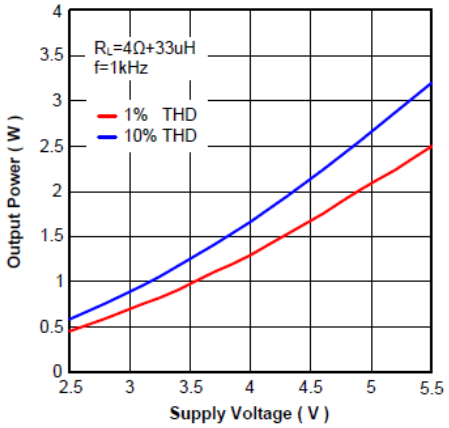
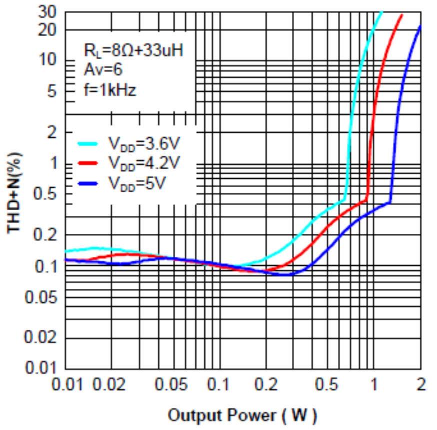


5. THD+N vs. OUTPUT POWER



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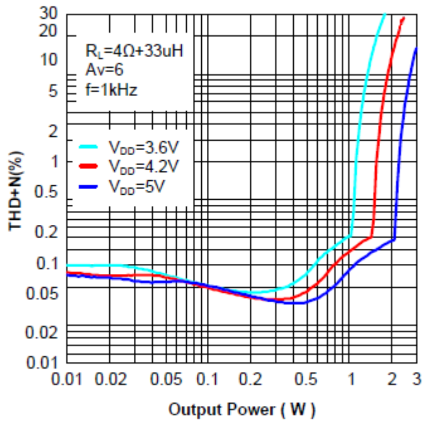
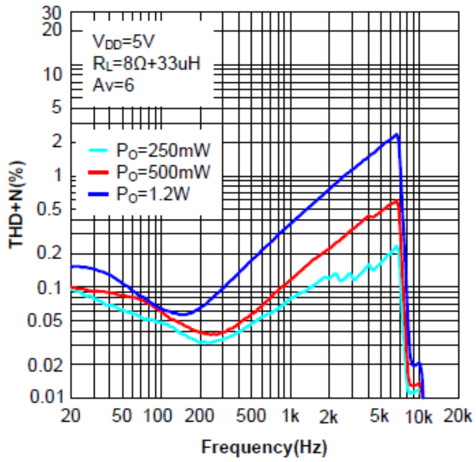


7. THD+N vs. FREQUENCY



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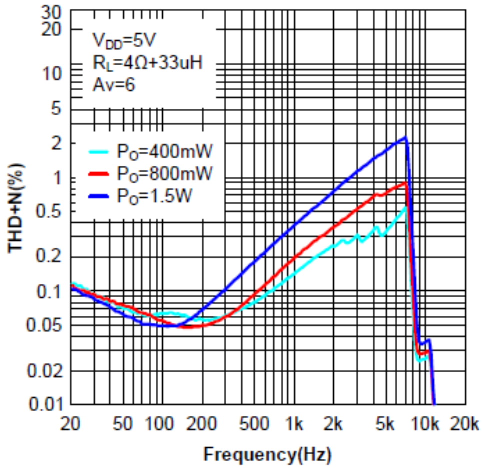
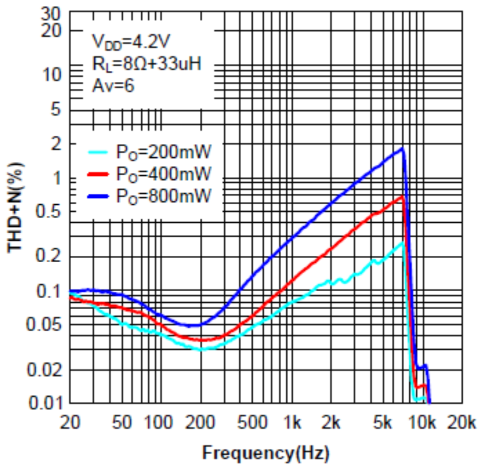
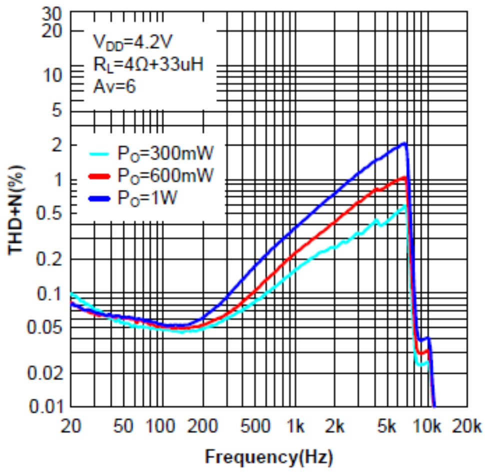


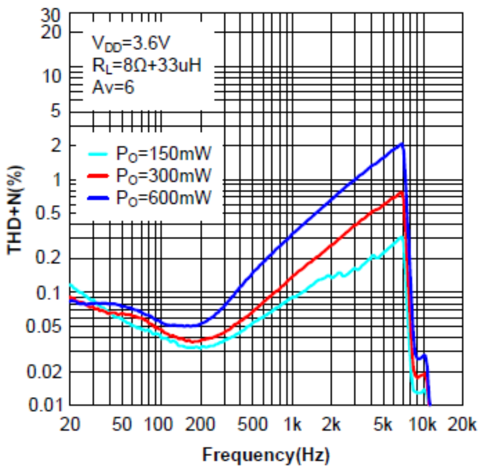
9. THD+N vs. FREQUENCY



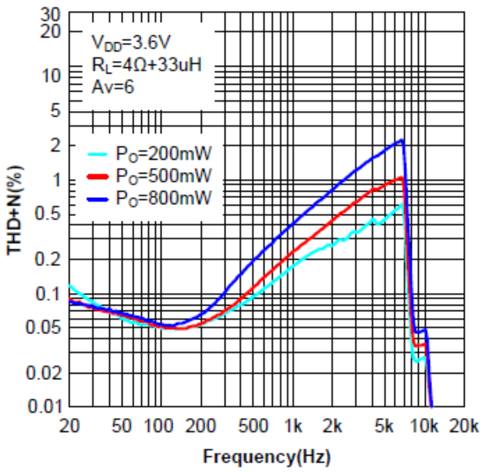
10. THD+N vs. FREQUENCY



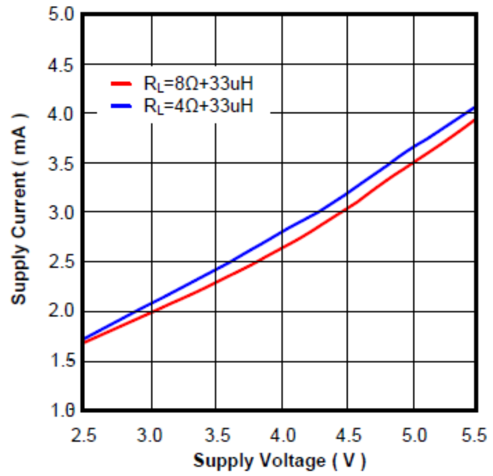
11. THD+N vs. FREQUENCY



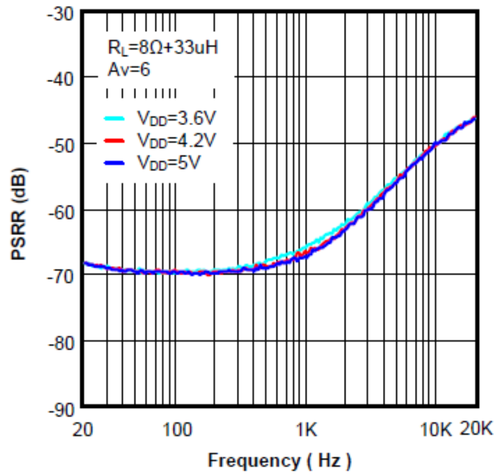
12. THD+N vs. FREQUENCY



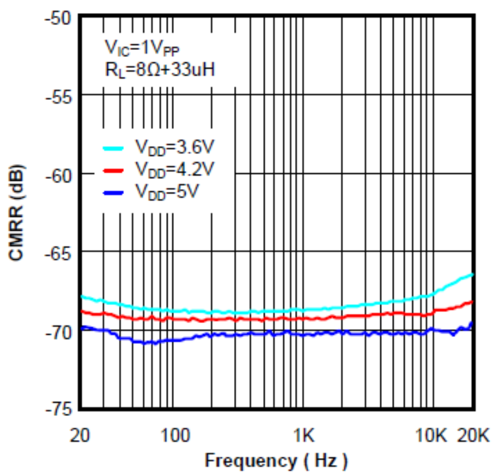
13. SUPPLY CURRENT vs. SUPPLY VOLTAGE



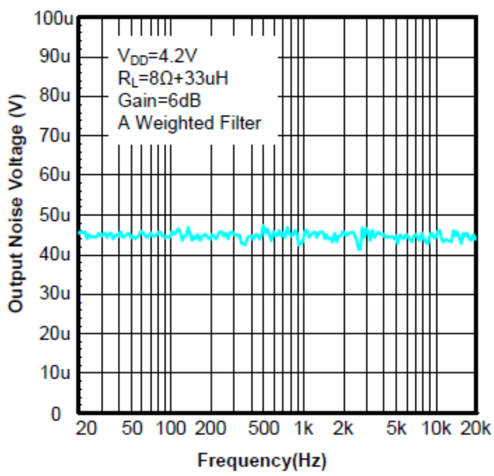
14. PSRR vs. FREQUENCY



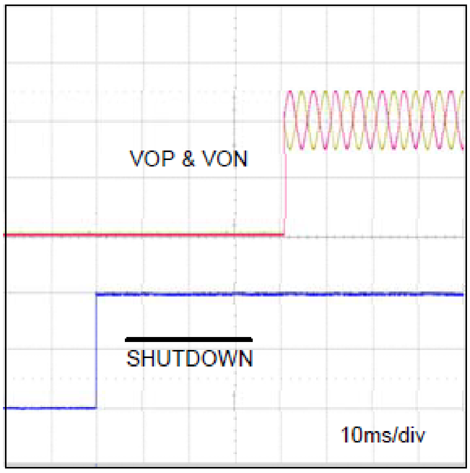
15. CMRR vs. FREQUENCY



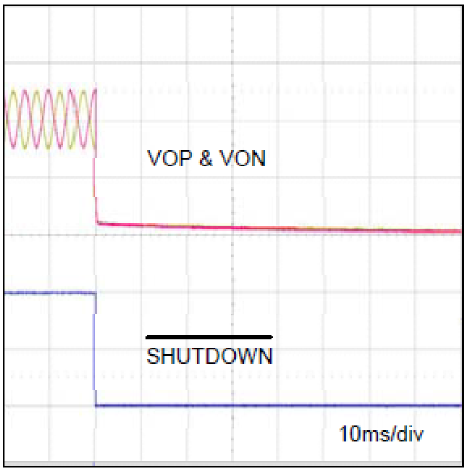
16. NOISE FLOOR



17. SYSTEM ON TIMING

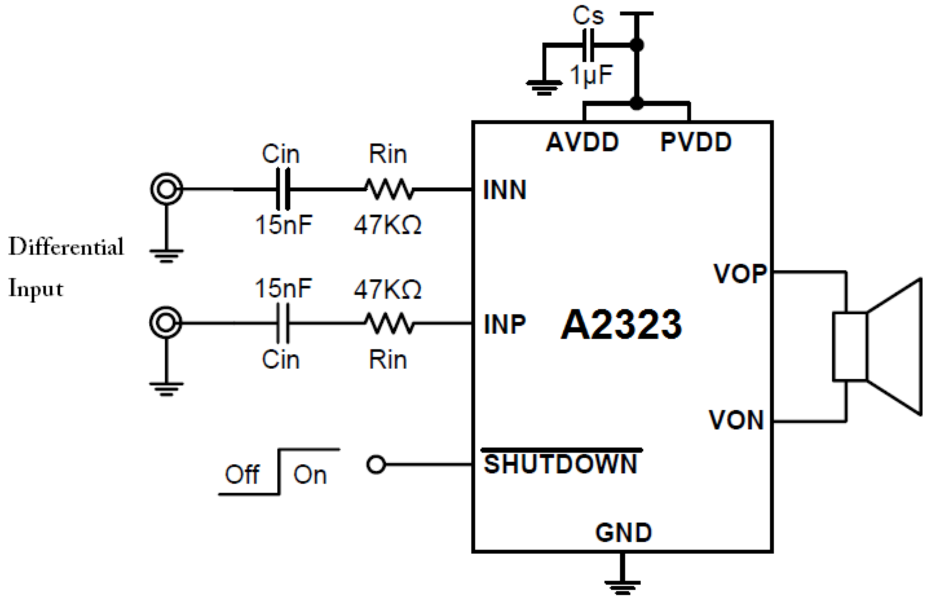


18. SYSTEM OFF TIMMING

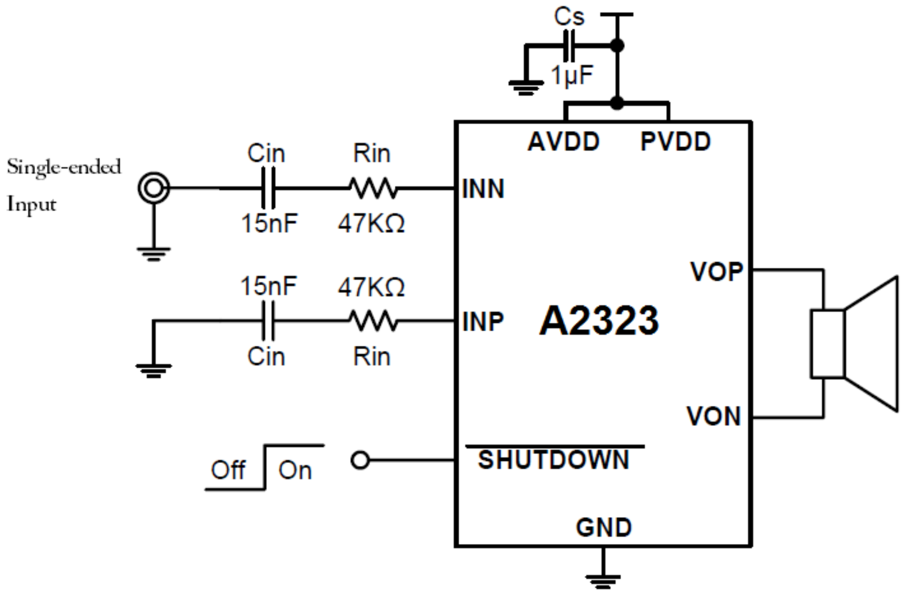


TYPICAL APPLICATION

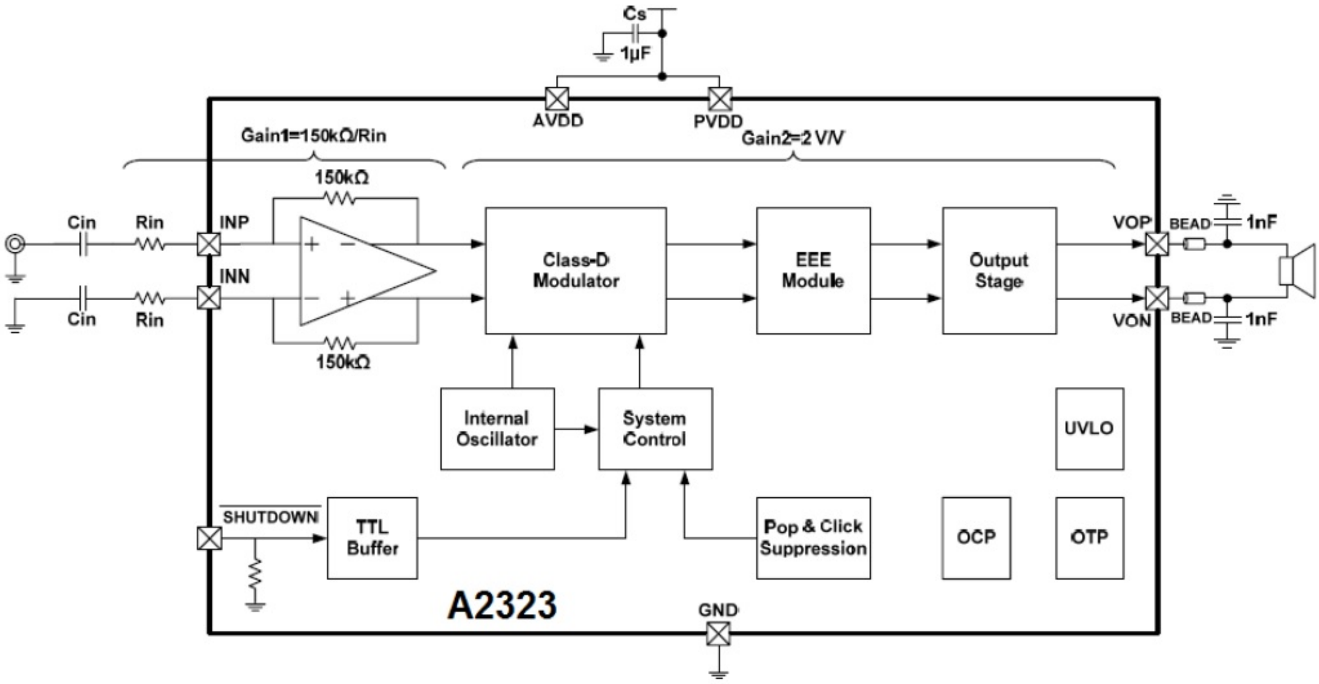
1. A2323 Differential INPUT application circuit



2. A2323 Single-ended INPUT application circuit



BLOCK DIAGRAM



Test Method

The A2323 is a class-D power amplifier, which the output wave form was modulated by the PWM square wave signal. The output port of the power amplifier can be connected with audio signal filter to filter out the PWM switching frequency energy between the test, obtain Intuitive analog output signal convenient for analyzing, both differential output port signal loaded to the speaker audio driving signal. The audio filter can be design by either the AP professional audio analyzer, or simple RC filter, as figure 1.

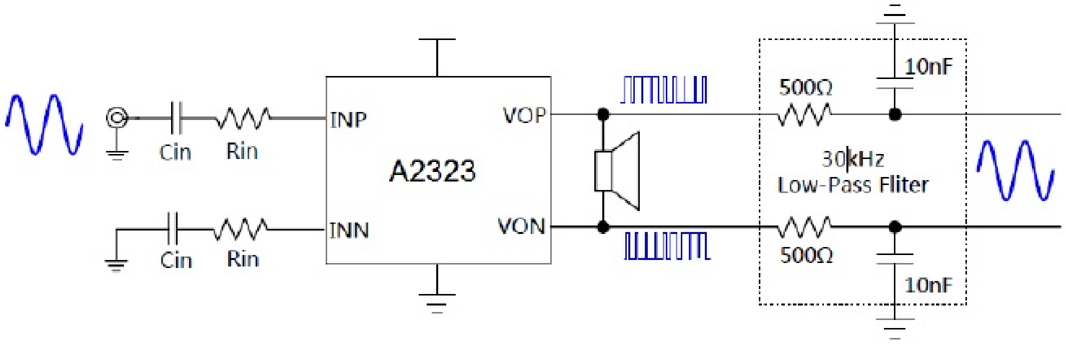


Figure 1 A2323 Testing Circuit Schematic

Low PASS Filter

Recommended low pass filter resistor, capacitor as below table.

Filter Type	Filter Resistor	Filter Capacitor	Low Pass Cut off frequency
RC Filter	R :500Ω	10nF	32kHz
	R: 1kΩ	4.7nF	34kHz

A2323 recommended filter for test

Power Gain calculation

According to the above testing method, an differential signal obtain form the low pass filter output port, using The oscillation scope to testing the effectively differential analog signal level VO_rms, as Figure 2.

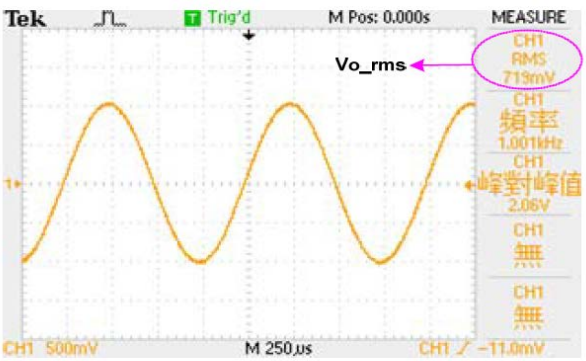


Figure 2 Effectively output signal diagram

The power gain of the power stage to speaker is calculated below: (RL is the speaker load impedance)

$$P_L = \frac{(Vo\_rms)^2}{R_L}$$

Operation Theory

The A2323 is Dedicated TDD suppression, super low EMI, single channel, class-D audio power amplifier. The dedicated RNS (RF-TDD Noise Suppression) technology, superior suppression in RF jamming when cellular Phone hands-free circuit power conducting and free space radiation, can effectively preventing TDD noise source. The A2323 dedicated EEE (Enhanced Emission Elimination) technology, reducing great level of EMI jamming in full frequency span range, for 60cm audio cable, over more than 20dB level in FCC standard.

The A2323 internal professional timing control circuit, fully Suppressed the “Pop-Click” sound, can effectively Erase the transient noise during power up, power down, power recovery and power off in system operation.

The A2323 internal over current protection function and thermal shutdown protection function, effectively protected chip operation form abnormal damage condition, when abnormal condition erase, it can recovery automatically.

The A2323 provide tiny 1.5mmX1.5mm FC-9 package, operating temperature range from -40℃ to 85℃.

RNS (RF-TDD noise Suppression)

TDD Noise origin source:

The GSM cellular phone is using the TDMA (Time Division Multiple Access) time slots sharing technology.

The time slots addressing divided each time to periodical frame, each frame divided into many time slots for Responding signal from base station, base station transmitting prearranging scheduled time slots signal to mobile terminal. Each of all these TDMA frames having 8 time slots, the frame periods between 4.615ms, each time slots periods between 0.577ms.

The standard GSM cellular phone, RF power amplifier transmitted signal each 4.615ms (217Hz), it will generated periodical burst current and strong radiation. Periodical burst current will created 217Hz power wavering; The 900MHz or 1800MHz high frequency RF signal generated 217Hz modulation radio frequency. The 217Hz power wavering will transmitted to audio signal channel through coupling, but the 217Hz modulated radio frequency signal coupled to audio signal channel through radiation, if lacking better protection mechanism, then the auditable TDD noise present, which include 217Hz noise and 217Hz harmonica noise signal.

The RNS technology suppressed the transmission and radiation interference through a comprehensive circuit structure, effectively increased TDD noise suppression capability.

Conducting Noise Suppression

The RF power amplifier operating, abstracting battery current form 217Hz frequency, due to the internal battery impedance, which will caused 217Hz power wavering, power wavering will passed the audio power amplifier through coupling to speaker. The capability of power wavering suppression depends on the audio power amplifier PSRR.

$$PSRR = 20\log\left(\frac{VOUT_{AC}}{VDD_{AC}}\right)$$

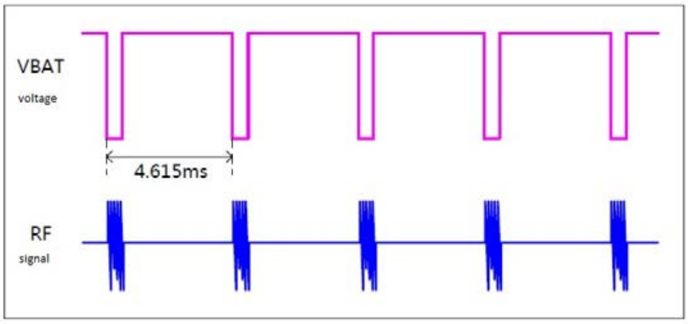


Figure 3 Diagram of power voltage and RF signal when GSM operating in Radio Frequency

As full differential amplifier input, output complete complement, theoretical the effect of power wavering related to the two output signal is the same, the differential output was not affect by the power wavering completely. In real situation, affect by the manufacturing defect cause, the power amplifier will mismatch in great deal, the PSRR are greater than -60dB, the -60dB represent 1000 decade of the output signal related to power wavering, for example of 500mVp power wavering, differential output signal will be 0.5mV, basically satisfied the need of application. But in the real world application, the PSRR -60dB even -80dB power amplifier could encounter conducting TDD noise problem, this is why? We still need to consider the mismatched impedance effect of the audio power amplifier component in this point. For the traditional audio power amplifier, as input resistance Rin, input capacitor Cin mismatching, affected greatly to audio power amplifier PSRR index. Consider resistance deviate between ±1%, capacitance deviate between ±10%, even the power amplifier performance is complete idea in this moment, the hole audio system PSRR theoretical level remain -30dB no more, affected deeply degrade conducting TDD suppression capability. While power wavering enhance, easily caused auditable TDD noise. For increasing the audio power amplifier PRSS at the input resistance, the input capacitance under mismatched condition, A2323 designed with special conducting noise reduction circuit, which can maintain highly PSRR level when the input resistance, the input capacitance deviated 10% even more that condition, greatly suppressed conducting noise source.

Radiation noise suppression

The input audio signal module layout, output audio signal module layout, speaker driving loop, even the power net and ground plane could be affect by radiated RF jamming, longer input net layout, output net layout resembled antenna effect, especially easy affect by RF radiated effect. The reasonable PCB layout design reducing radiated RF effect, like shorten input net layout, output net layout length; The audio circuit component stayed away from RF antenna as far as possible and keep shielded from RF antenna; Maintain all the audio signal channel component integrity; Connect small capacitor to ground in sensitive point to bypass RF signal. But in practical application, PCB layout hardly full scale evaluate the effect from radiated RF to audio signal channel, however some RF energy coupling through audio signal channel, become the auditable TDD noise. The A2323 design with special radiated RF suppression circuit internally, created mask shielding inside the chip, effectively brocaded High frequency RF energy penetrating the chip, guarantee the power amplifier speaker output driven signal in affect by antenna RF radiated effect, finally avoided TDD noise from antenna radiated RF.

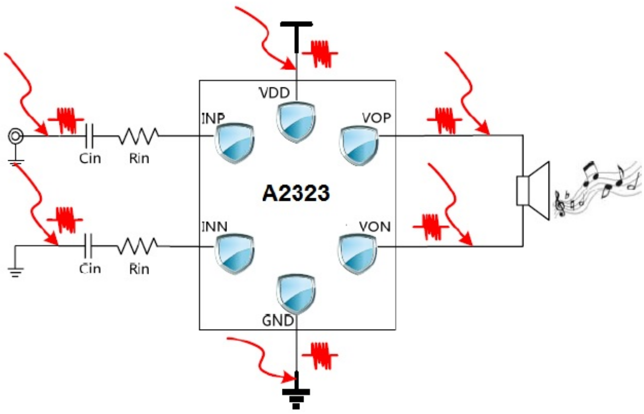


Figure 4 Diagram of radiated RF

Filter Less

The A2323 designed with filter less PWM modulation, cut tradition class-D power amplifier LC filter, enhance the efficiency, provided smaller size, and contributed better cost effect solution.

POP-Click sound suppression

The A2323 embedded with dedicated timing control circuit, present complete the Pop-Click sound suppressed, effectively erased system power up, power down, power weak and power off operating transient noise.

EEE technology

The A2323 design with dedicated EEE technology, engaging full scale in High Frequency transient skipping signal, reduced great level EMI jamming in full frequency span range. For 60cm audio cable, over more than 20dB level range in FCC standard, as figure 5 diagrams.

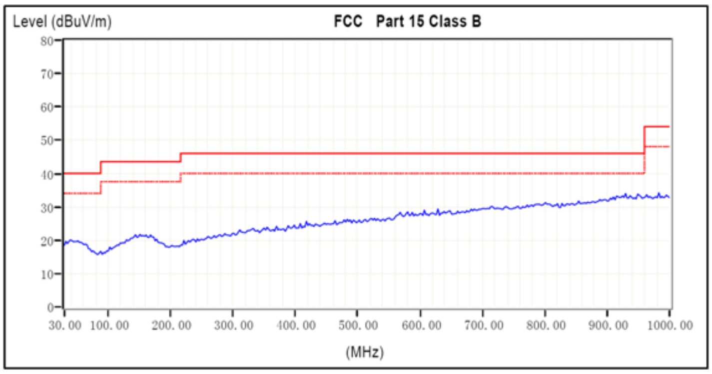


Figure 5 EMI Diagram of testing frequency spectrum

Efficiency

The switching way of output transistor decided the high efficiency of class-D power amplifier. In class-D power amplifier, the output transistor acting like a current switching regulator, basically switching consumption power can be neglected in switching process. The main consumption power is generated by the MOSFET conducting resistance and the I^2R created by Power source current. The A2323 efficiency can be achieved 90%.

Automatic protection recovers

While the output pin short with main power or ground, or short between the output lead, over current protected circuit will shut off the chip for preventing damage. After recovery from shorting circuit, the A2323 was operating automatically. When the chip operating temperature over the thermal shut down temperature threshold(160℃), the chip will be shut down. When the operating temperature down to recover temperature threshold(125℃), the A2323 continue to operating normally.

Application Information

Power decoupling capacitor

Excellent power decoupling capacitor can increase power amplifier efficiency and transient characteristic, low ESR (equivalent-series-resistance) ceramic capacitors X5R or X7R are recommended. Usually recommended connecting 1uF and 33pF two decupling capacitors to bypass VDD to ground, decupling capacitor 0.1uF can grantees power amplifier low frequency transient response, but smaller capacitor 33pF filter out power source radiated RF jamming signal, because capacitor 33pF resonant frequency at RF frequency range, for 900MHz or 1.8GHz RF frequency jamming provide better filter characteristic. Meanwhile the decoupling capacitor layout should near the chip VDD layout as near as possible to achieved best filtering effect.

Input resistance

The A2323 is a full differential structure, designed by differential input and single-ended input, under both input condition, the input resistance remain the same; through input resistance design can calculate the gain of the amplifier, equation is below:

$$Gain=\frac{2x150k\Omega}{Rin}$$

All explanation stated that increasing the chip PSRR, CMRR, and THD characteristic by better matching between two input resistors, so recommended designing with 5% accuracy resistor or better resistor. While PCB layout, resistor should near power amplifier layout, it can prevent noise injecting into high resistance point.

Input capacitor

Between Input resistance and input capacitance become a high pass filter, the equation of cut off frequency as below:

$$f_C=\frac{1}{2\pi x\, RinCin}$$

The smaller CIN Capacitor helping filter out 217 Hz input coupling noise, and smaller capacitor decreased power amplifier power up Pop-Click sound. Better matching between two input capacitor increase chip total performance and suppressed Pop-Click sound, design 10 % accuracy resistor or better accuracy resistor is recommended.

Bead and Capacitor

The A2323 under lacking bead, capacitor condition, for 60cm audio cable, still can meet FCC standard. For lengthen audio output signal route and component near EMI sensitive device, design with bead, capacitor is recommended. The placement of bead and capacitor must as near as possible.

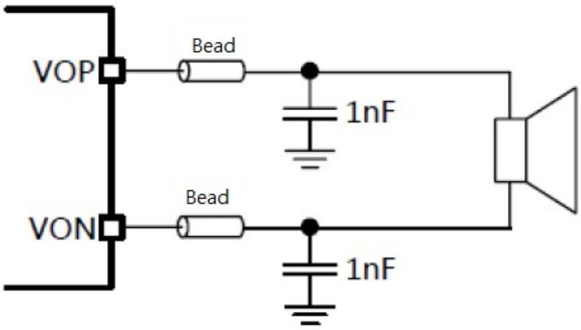


Figure 6 Bead and Capacitor

Bead Recommend Type

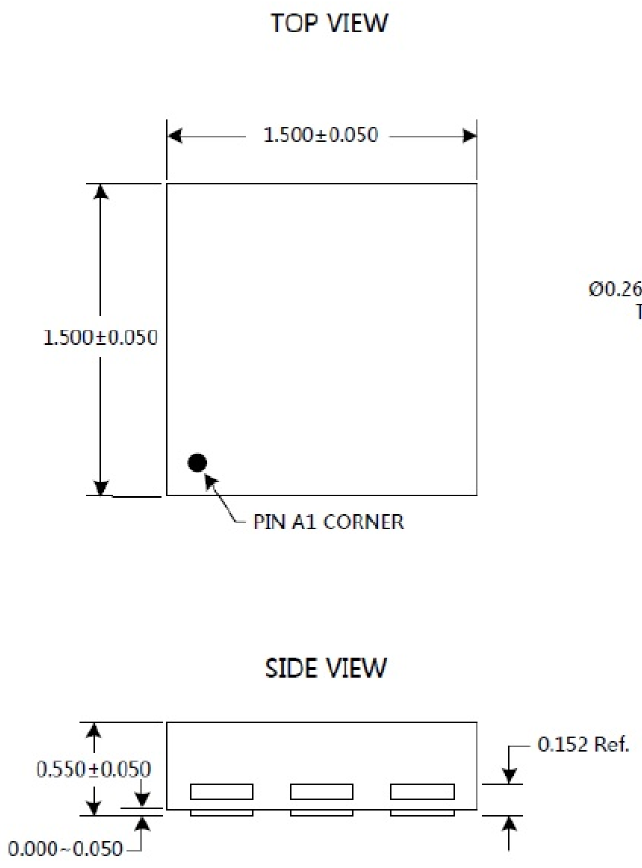
The A2323 as class-D power amplifier, output square wave signal, this square wave signal creating switching current under output filter capacitor, causing static power consumption, so bigger output filter capacitance not recommended, design with 1nF ceramic capacitor is recommended.

FC Package

The A2323 provide tiny 1.5mm X 1.5mm FC-9 package. The FC package base on advance Flip-Chip packaging technology, copper plated silver frame (Cu/Ag), Package pad with tin plated layer thickness between 0.03~0.05mm, capable of mature stable packaging reliability, it has been guaranty the surface mount process Yield rate.

PACKAGE INFORMATION

Dimension in FC-9 (Unit: mm)



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